Welcome To

ISSCC 2014 Session 17 Analog Techniques

An Integrated 80V 45W Class-D Power Amplifier with Optimal-Efficiency-Tracking Switching Frequency Regulation

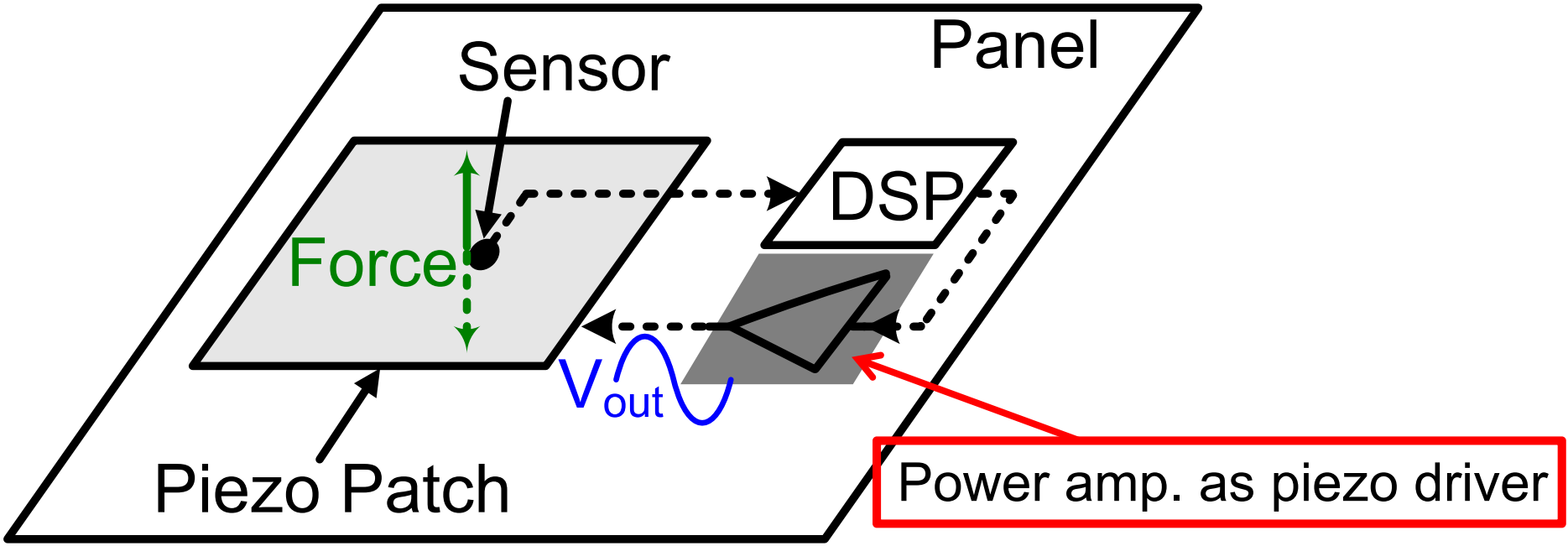
Haifeng Ma, Ronan van der Zee and Bram Nauta
IC Design Group , University of Twente
Enschede, The Netherlands

Outline

- Introduction
- Power Dissipation in Class-D Output Stages
- Switching Frequency Regulation for Optimal Efficiency
- Circuit Implementation
- Measurements
- Conclusion

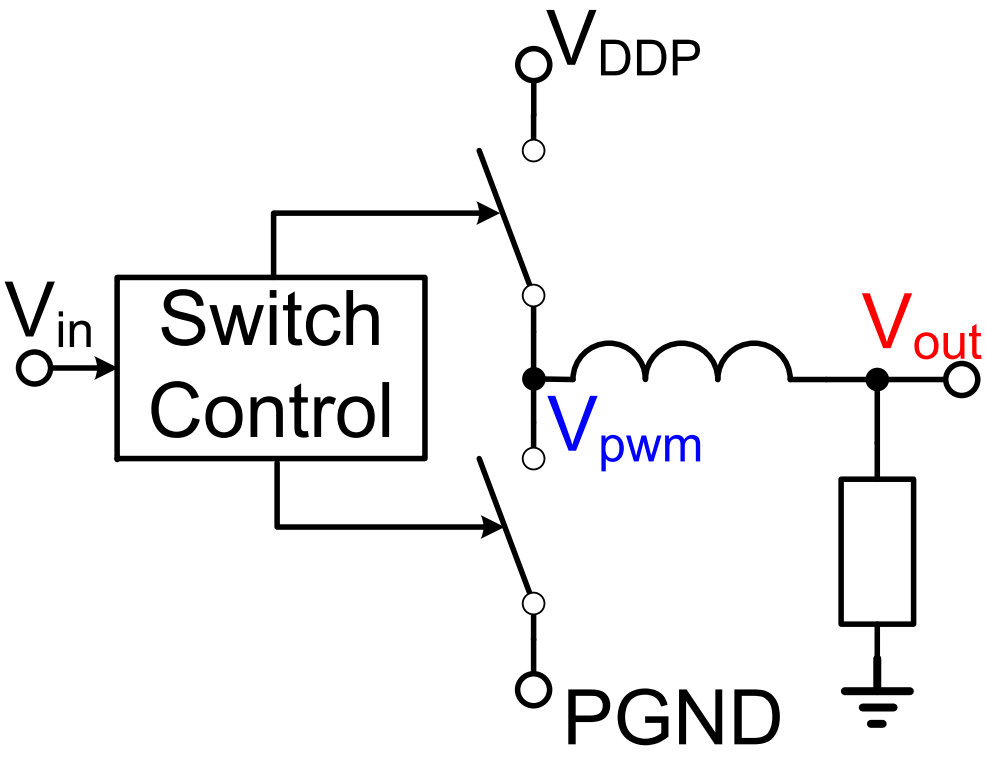
Introduction

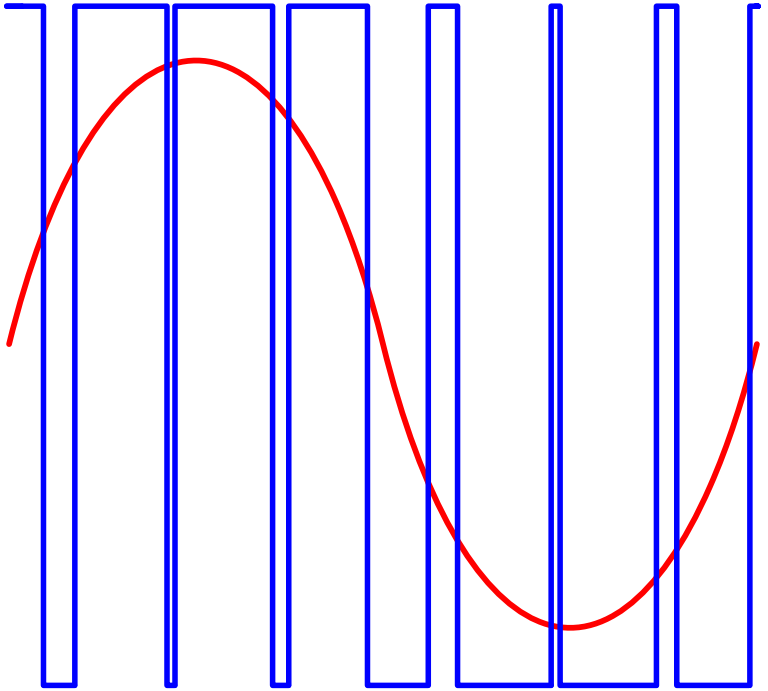
- Piezoelectric actuator loads
  - Active vibration & noise control
  - Signal frequency <1kHz
  - Capacitive, 100V, 1-100W reactive power



Class-D Amplifier

- High peak efficiency (typically ≈90%)
- Small or even no heat sink





Motivation

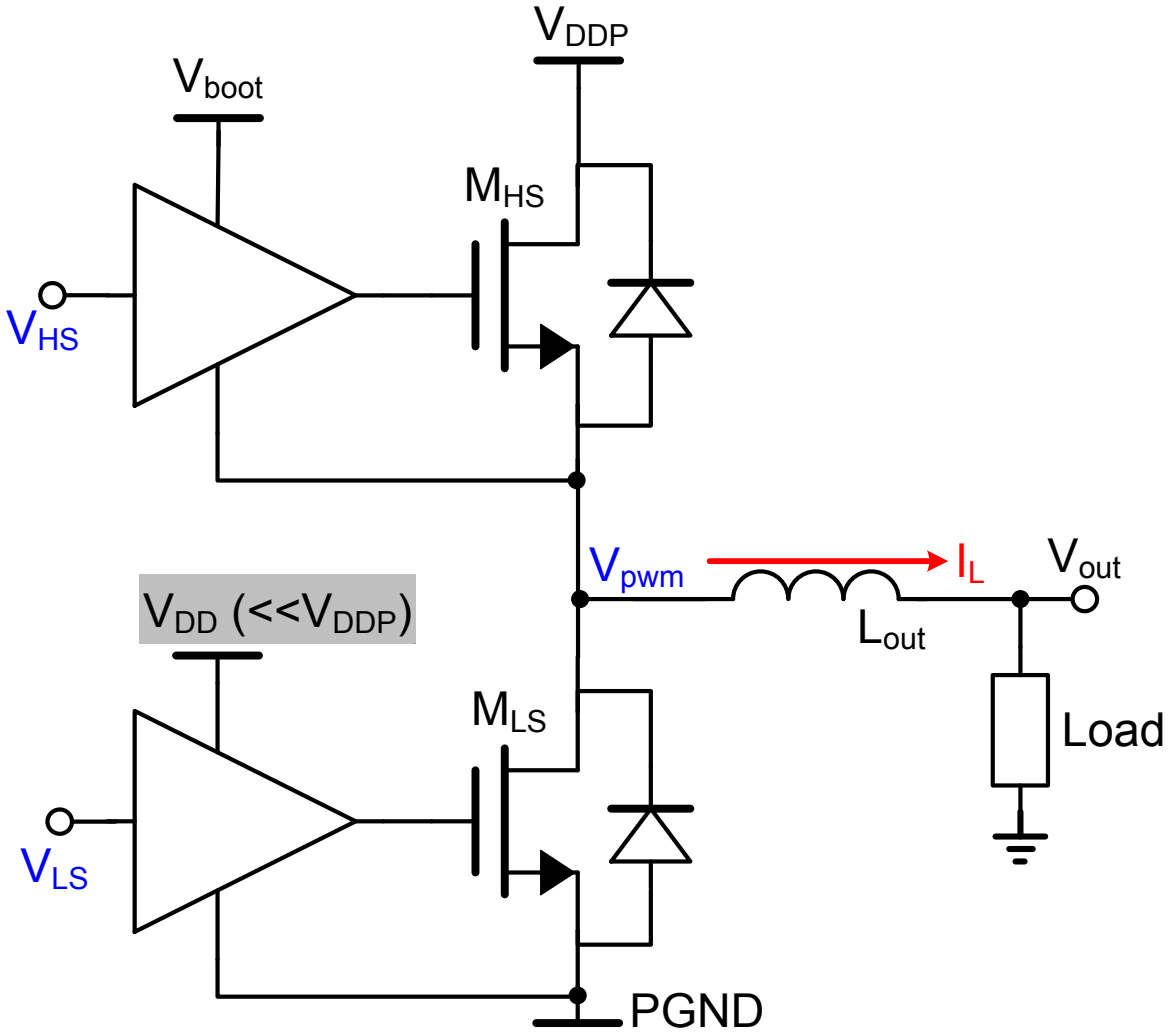
- 90% efficiency only at high output power
- Average P_{out} << Maximum P_{out}
- ➔ Obtain high power efficiency over the full output power range.

Outline

- Introduction
- Power Dissipation in Class-D Output Stages
- Switching Frequency Regulation for Optimal Efficiency
- Circuit Implementation
- Measurements
- Conclusion

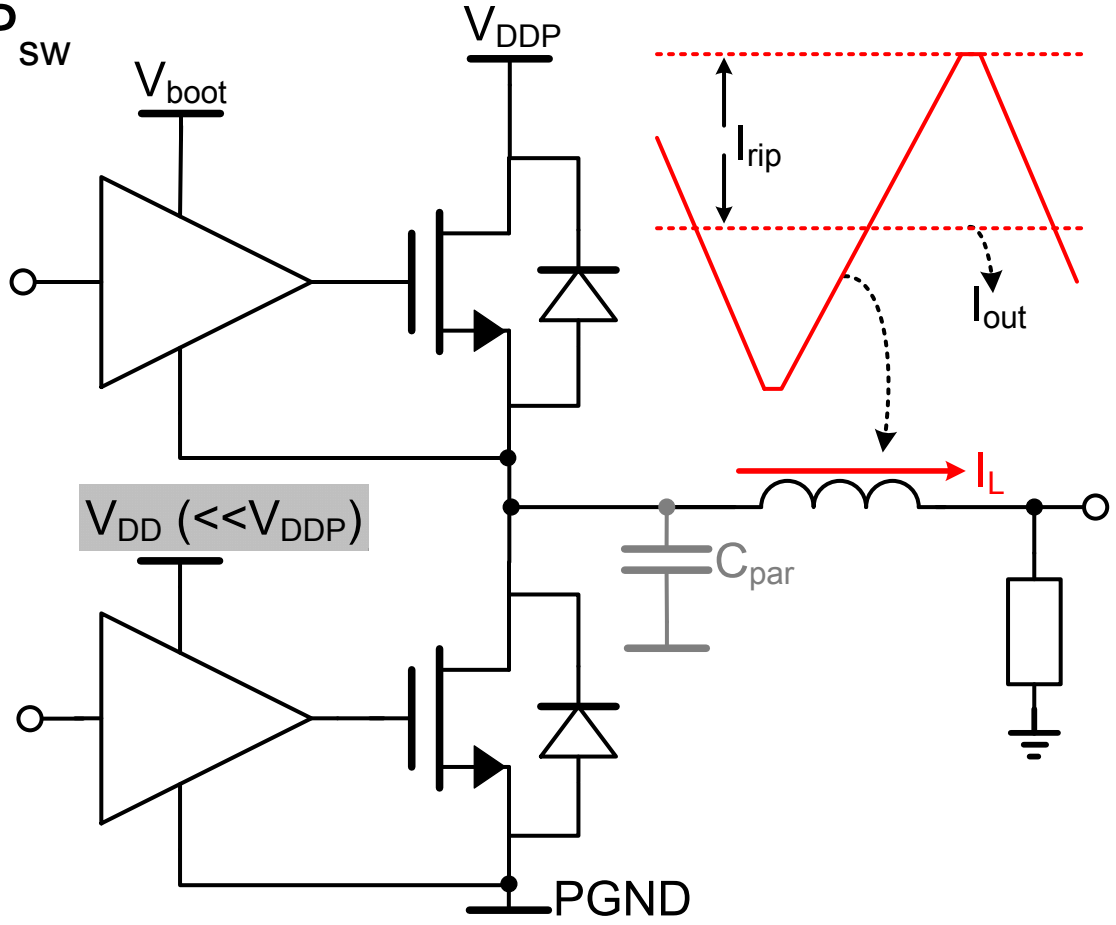
High-Voltage Class-D Output Stage

- N-type DMOS FETs as power switches
- $V_{DD} << V_{DDP}$



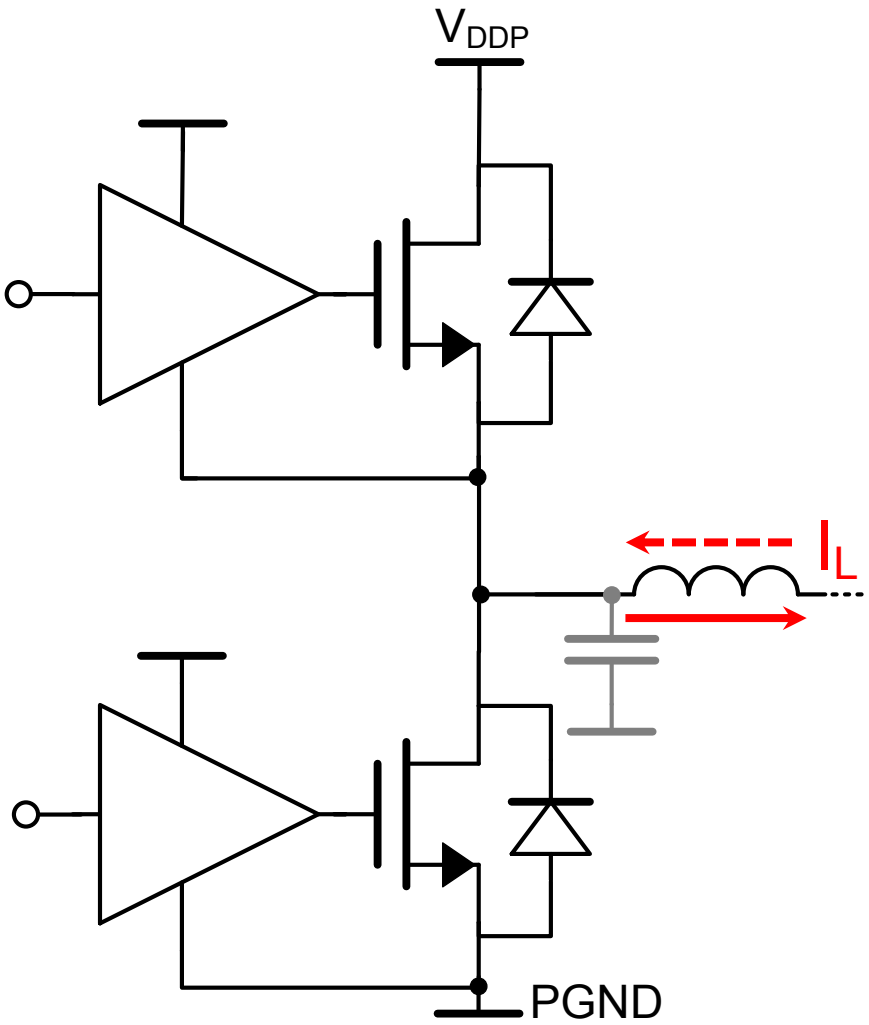
Power Dissipation Sources

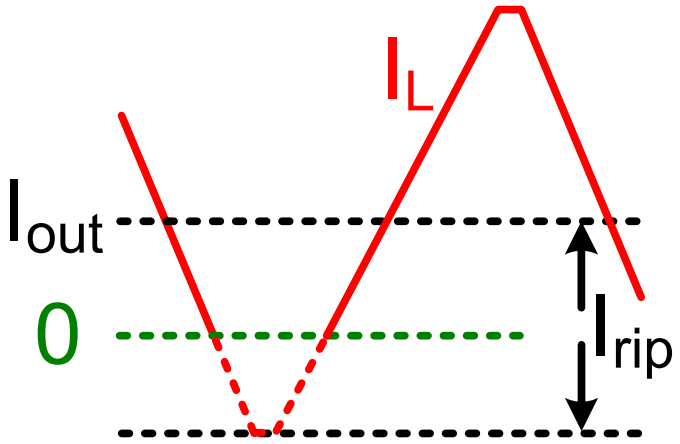
- Conduction loss P_{con} (I_{out} conduction)
- Ripple loss P_{Irip} (I_{rip} conduction & L_{out} core loss)
- Switching loss P_{sw}



Lossless Soft Switching (I_{rip}>I_{out})

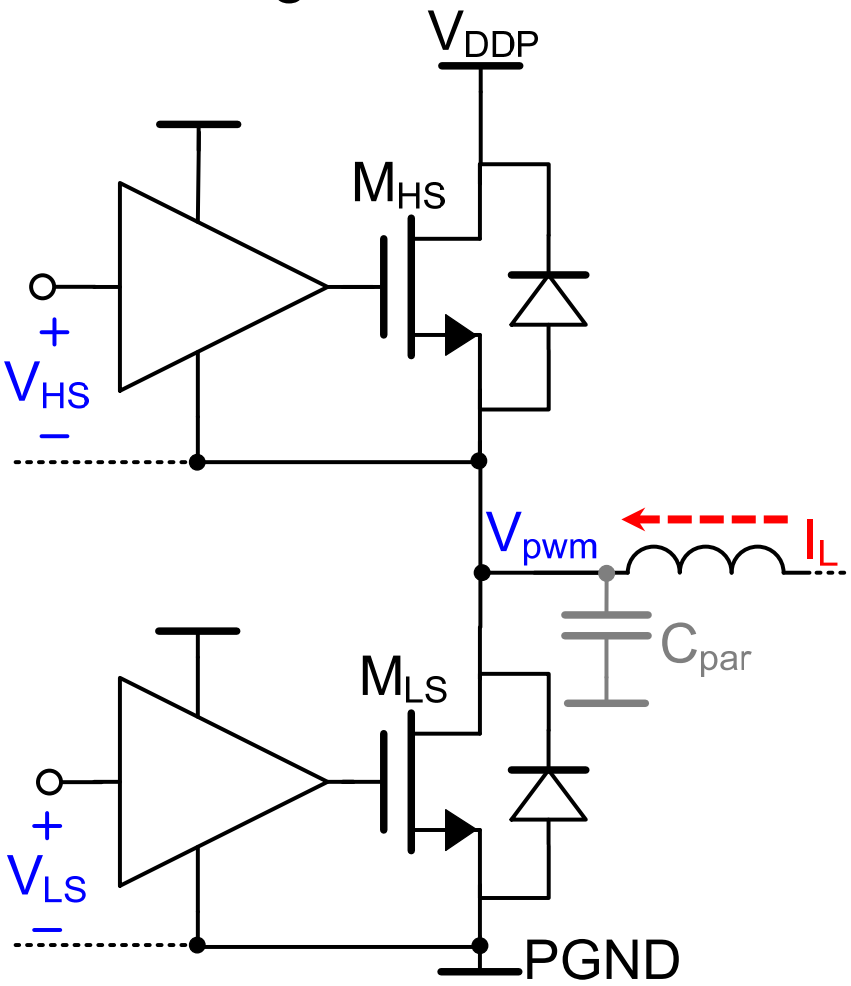
- Bidirectional inductor current I_L

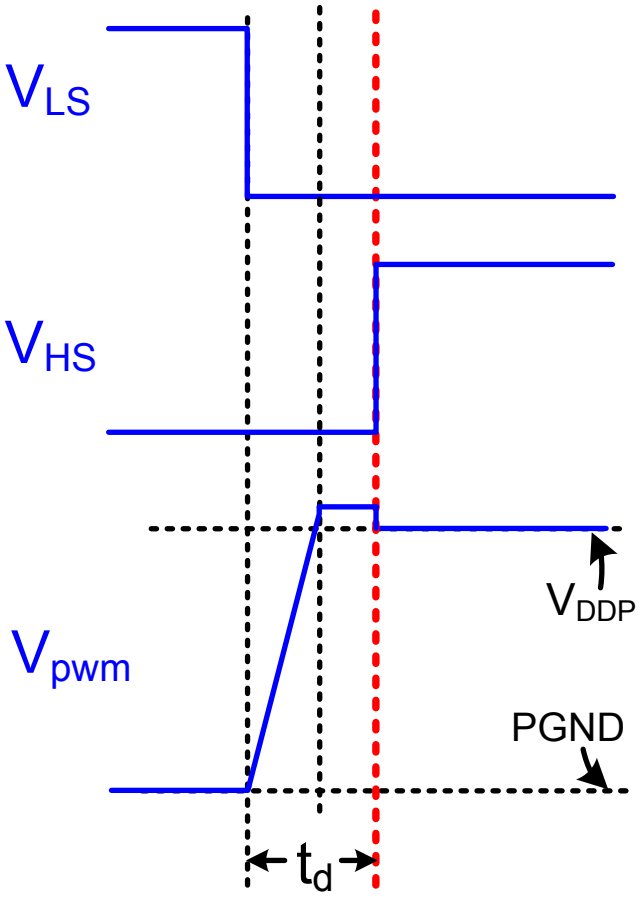




Lossless Soft Switching (I_{rip}>I_{out})

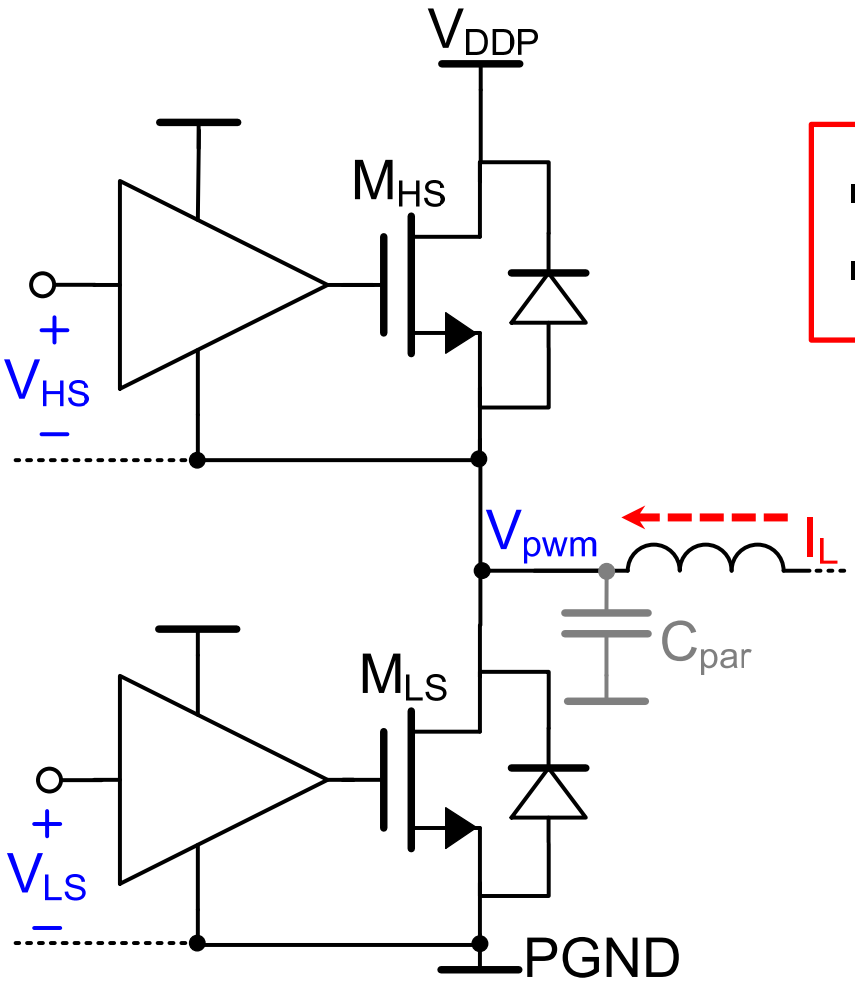
- Bidirectional I_L fully (dis)charge C_{par} ➔ Lossless soft switching





Lossless Soft Switching

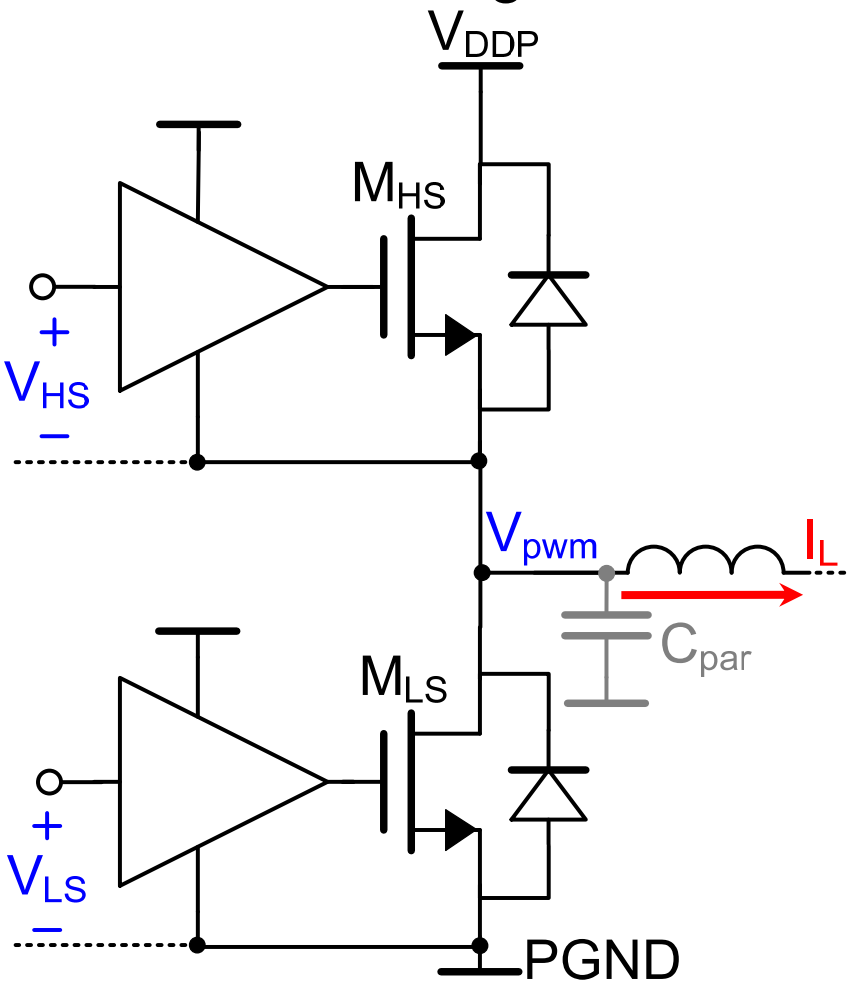
- Inductor ripple current $I_{rip} \propto 1/f_{sw}$

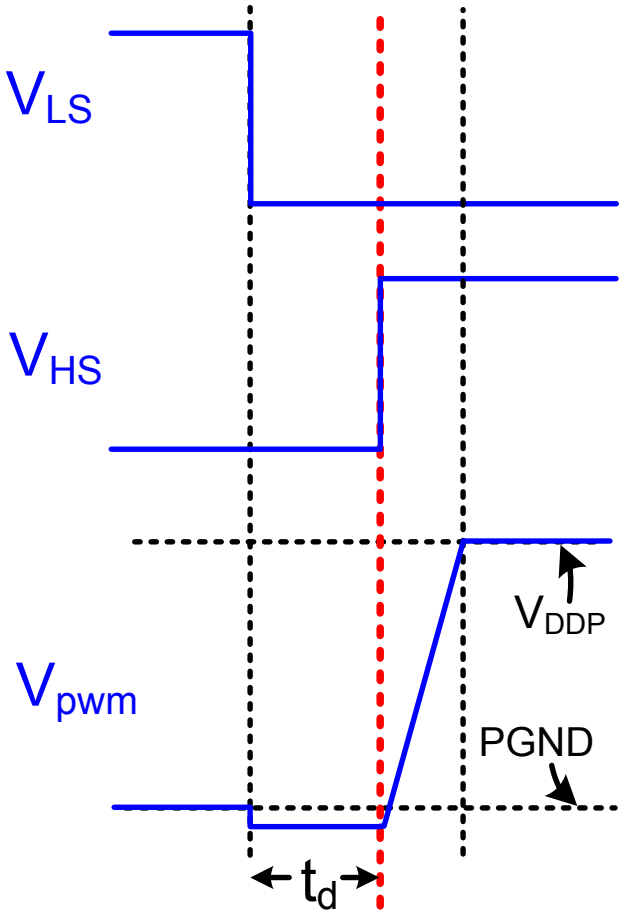


- P_{Irip} dominates at low P_{out}
- $P_{Irip} \propto 1/f_{sw}$

Hard Switching (I_{rip}<I_{out})

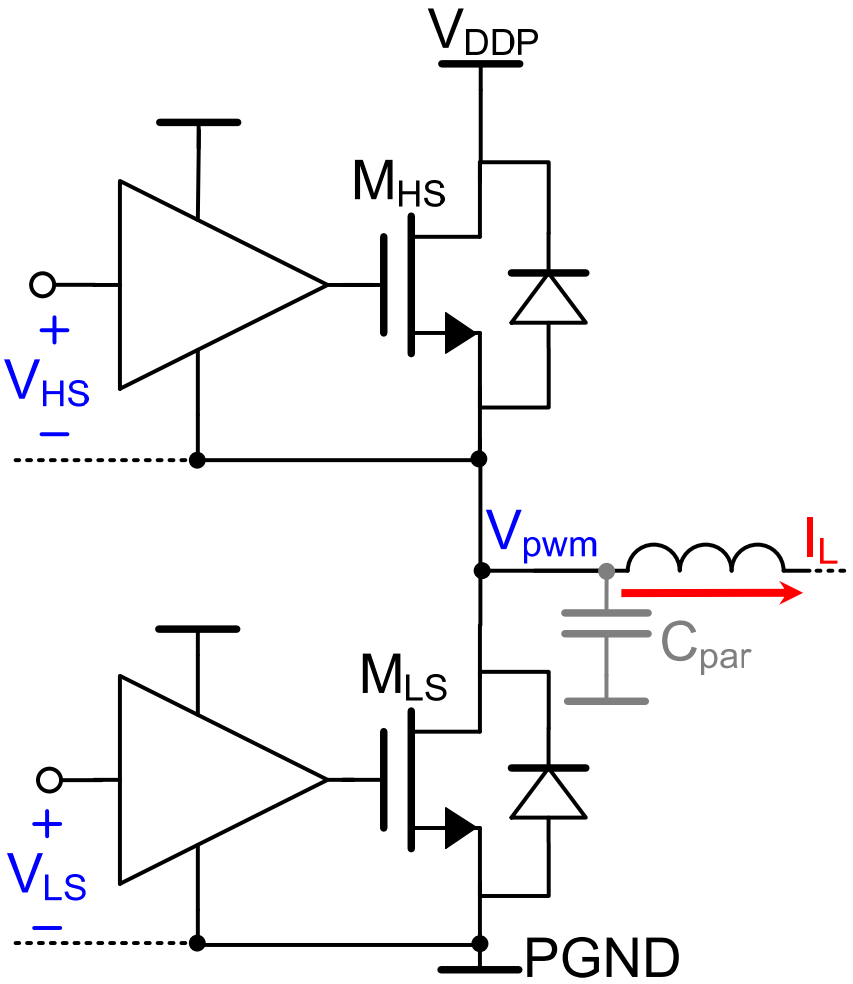
- Unidirectional I_L ➔ (Dis)charging of C_{par} done by $M_{HS(LS)}$ for one switching transition





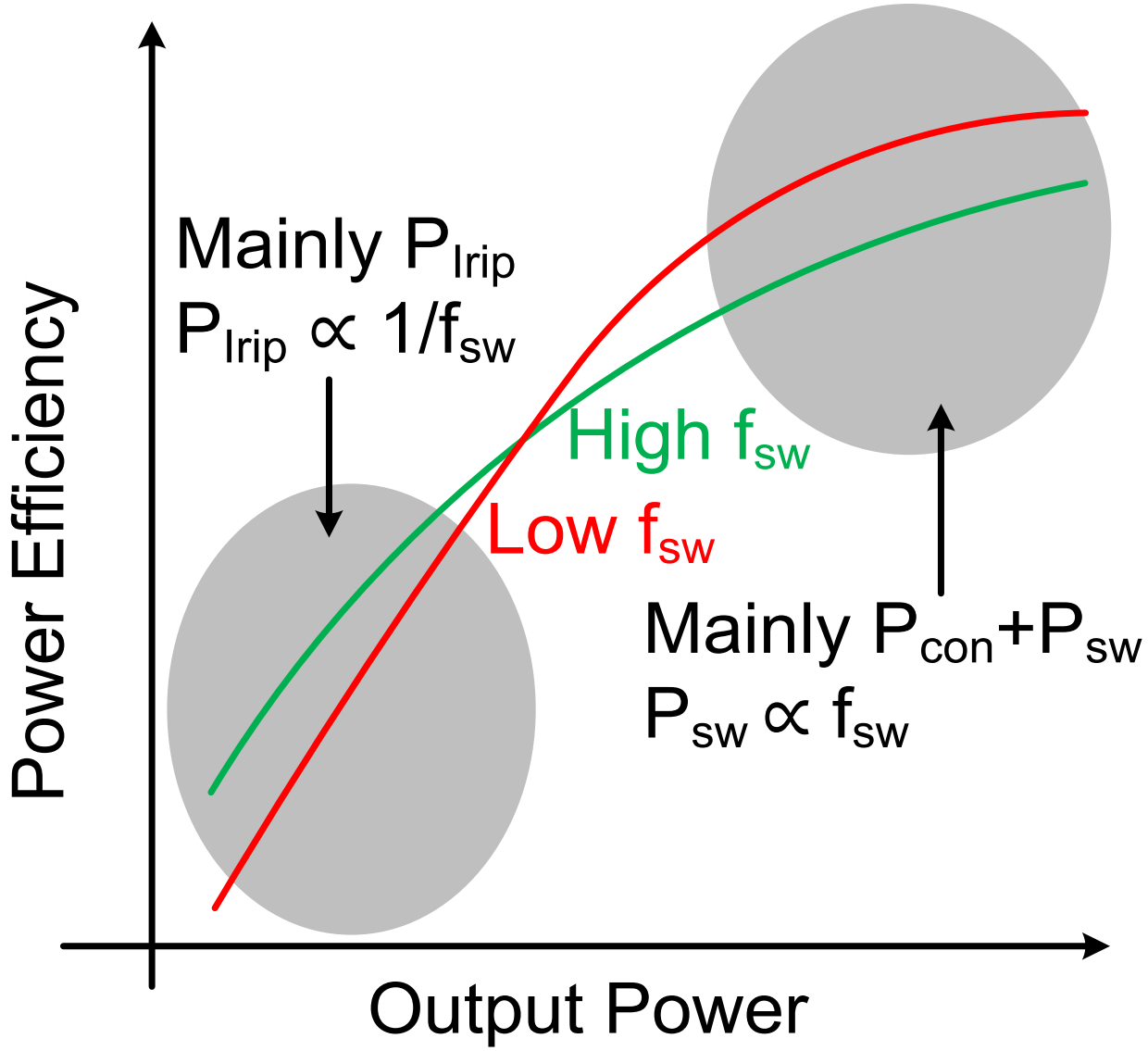
Hard Switching (I_{rip}<I_{out})

- High V_{DDP} ➔ switching loss P_{SW} significant



- Balanced P_{con} and P_{sw} dominates at high P_{out}
- $P_{sw} \propto f_{sw}$

Efficiency vs. Switching Frequency



Challenge and Objective

- Varying f_{sw} ➔ better efficiency
- Optimal f_{sw} depends on both I_{out} and I_{rip}.
- In class-D, I_{rip} changes a factor >5 in the 0.05-0.95 duty cycle range.

➔Find optimal f_{sw} in all situations

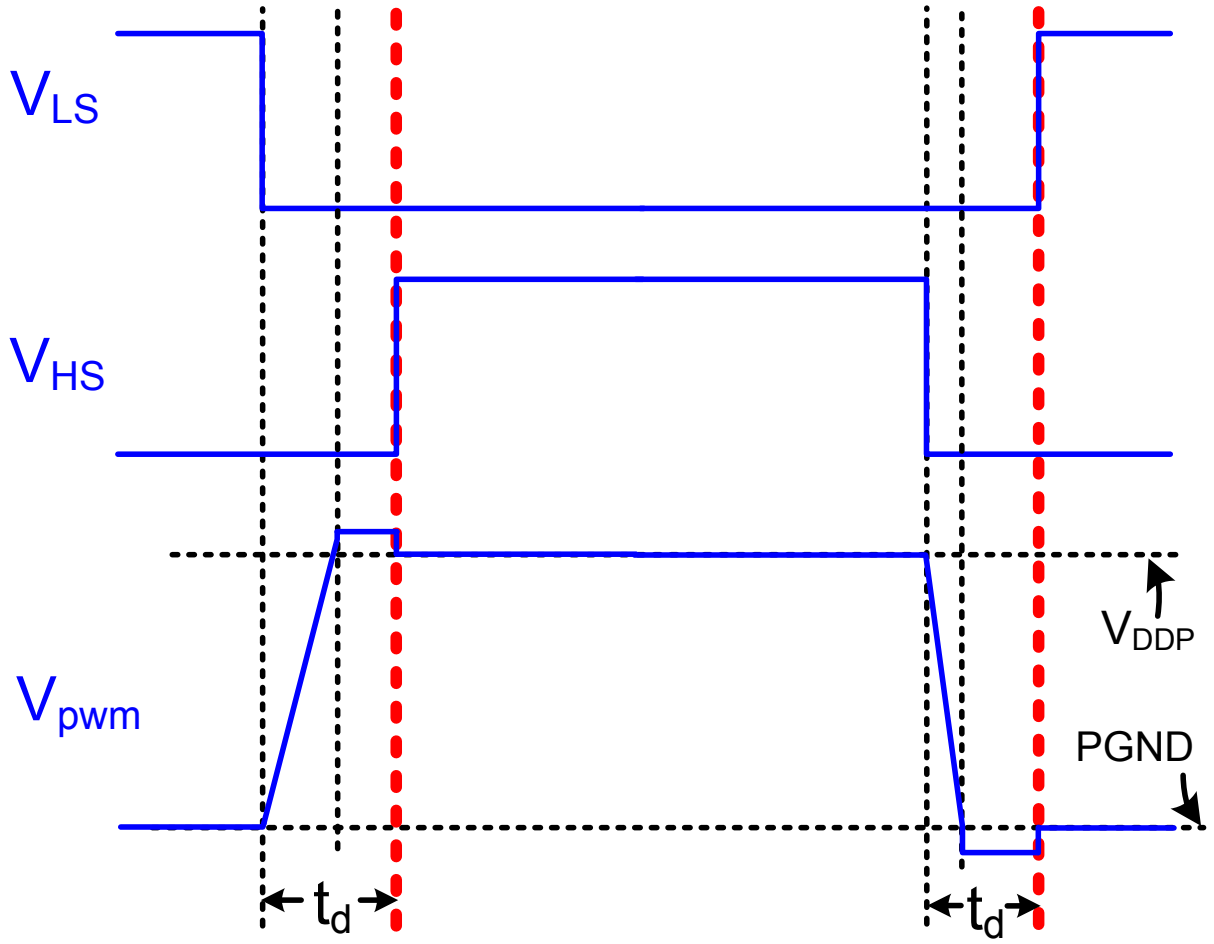
Outline

- Introduction
- Power Dissipation in Class-D Output Stages
- Switching Frequency Regulation for Optimal Efficiency
- Circuit Implementation
- Measurements
- Conclusion

Indicating Optimal f_{sw} by V_{pwm} Level (I)

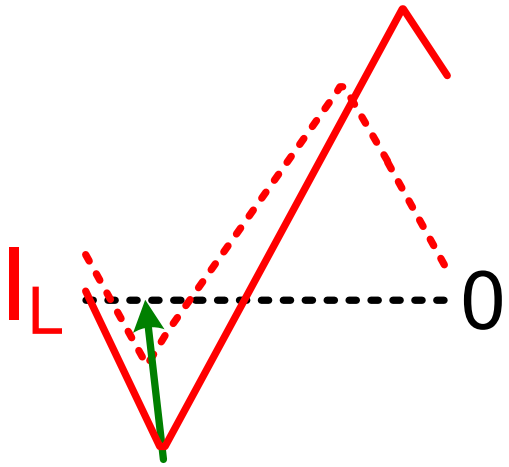
- Both V_{pwm} levels already at the other supply rail when M_{HS}/M_{LS} turns on

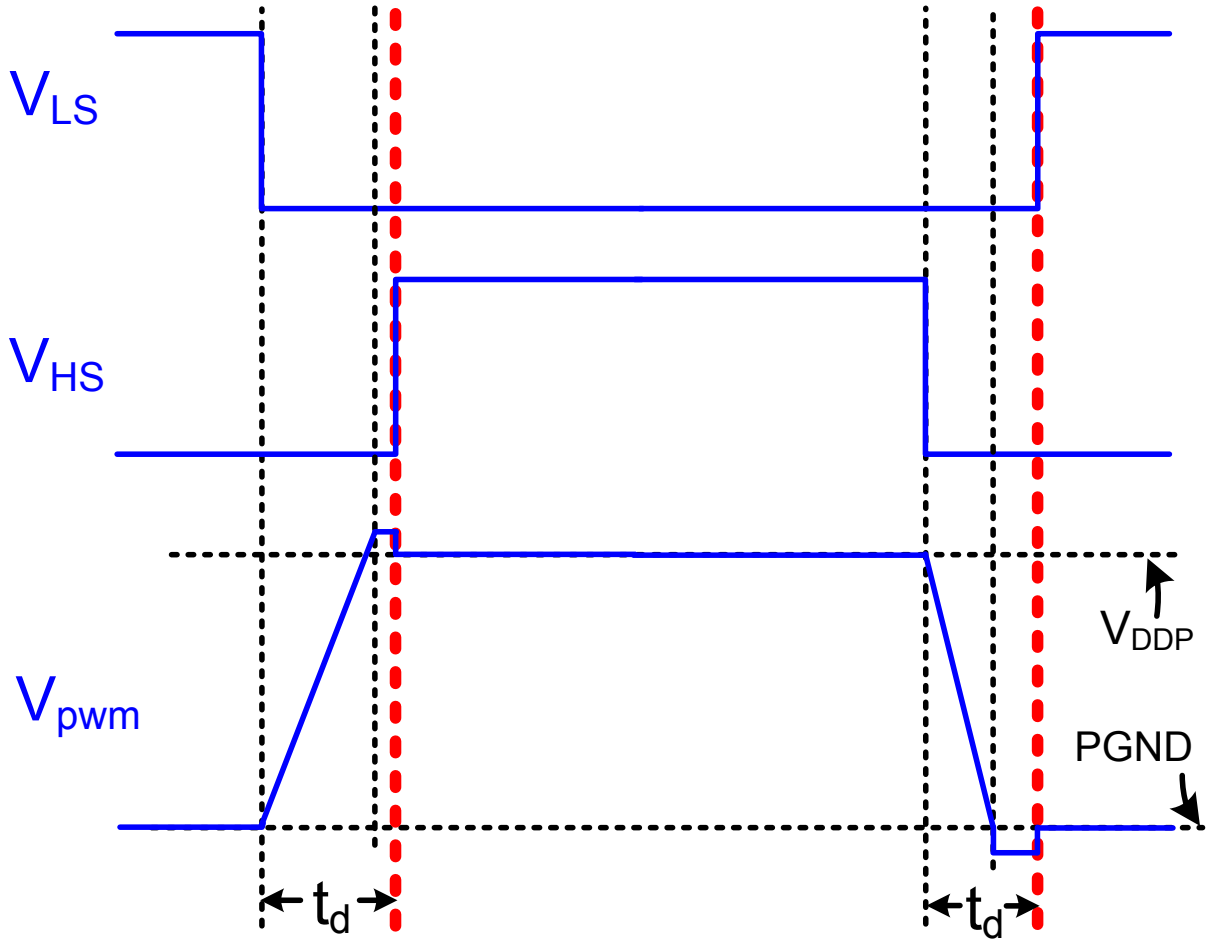
No P_{sw} ➔
Increase f_{sw} to minimize P_{Irip}



f_{sw} Influence on V_{pwm} Transitions

- Increase f_{sw} ➔ V_{pwm} transitions become slower

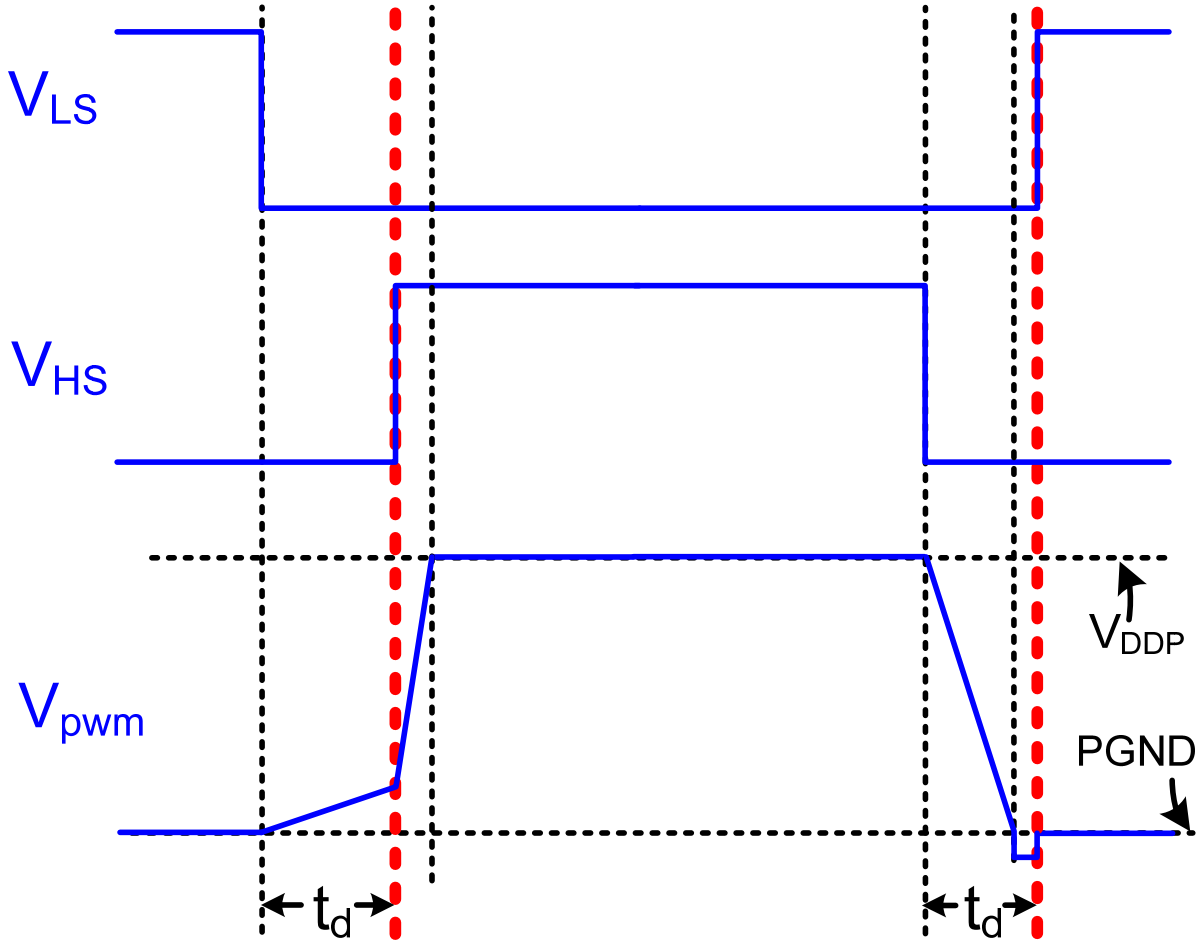




Indicating Optimal f_{sw} by V_{pwm} Level (II)

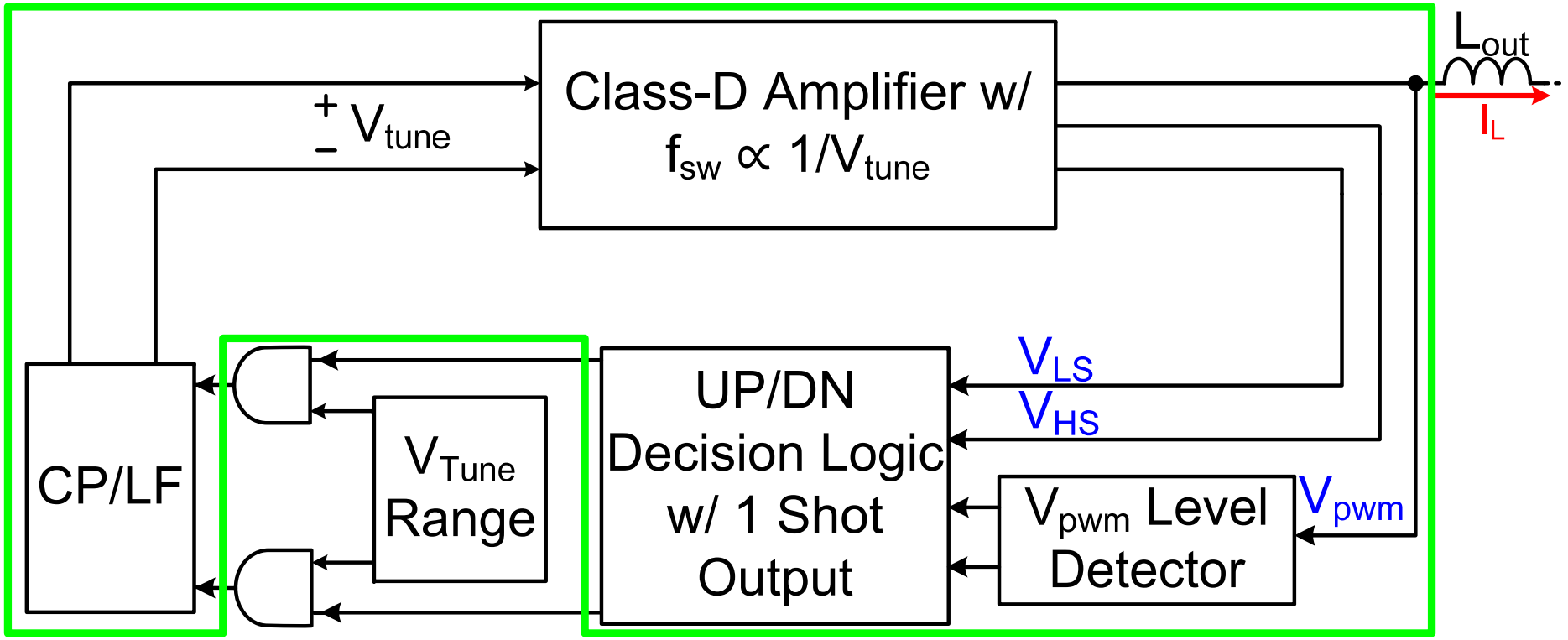
- Either V_{pwm} level not yet reached the other supply rail when M_{HS}/M_{LS} turns on

P_{sw} exists➔ Decrease f_{sw} to minimize P_{sw}



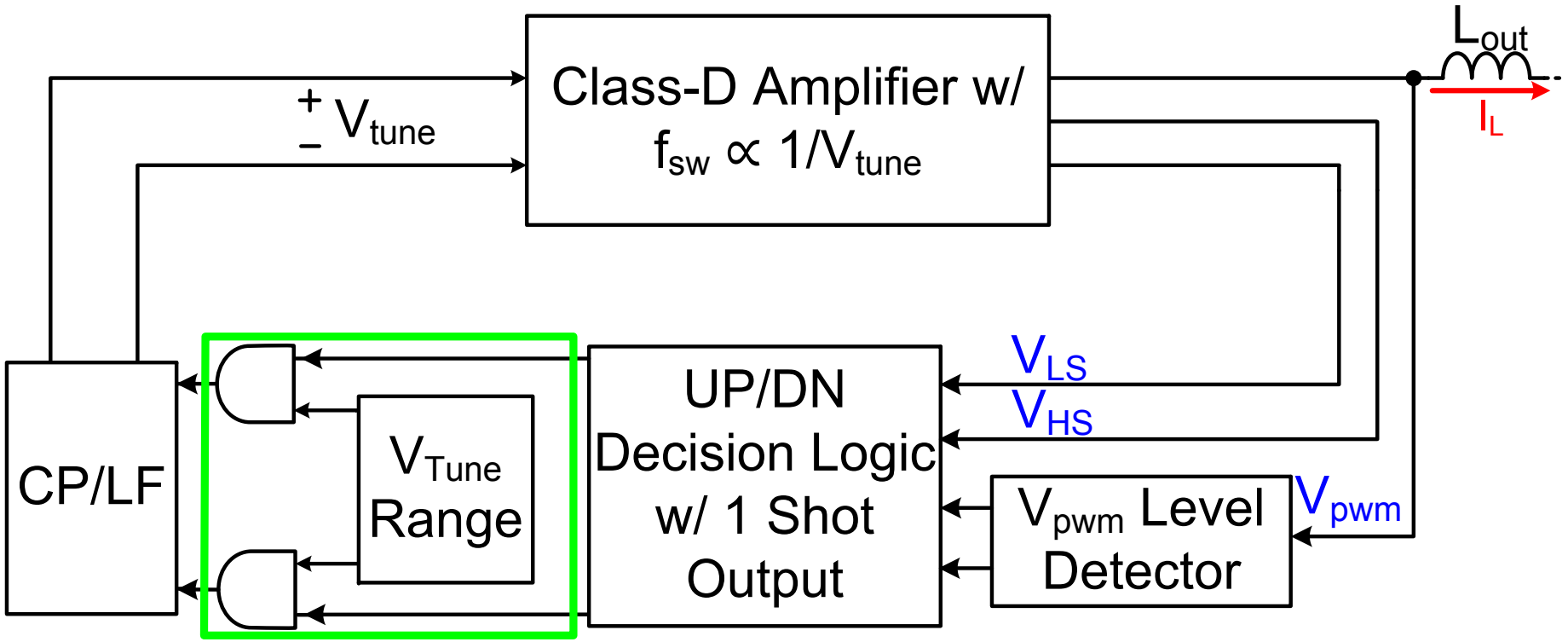
Switching Frequency Regulation

- Adapting f_{sw} ➔ either one of the V_{pwm} switching event is at the boundary of being lossless while the other is fully lossless



Switching Frequency Limit

- Setting f_{sw} lower limit ➔ the system naturally shifts to hard switching at high output power, with minimized P_{sw}

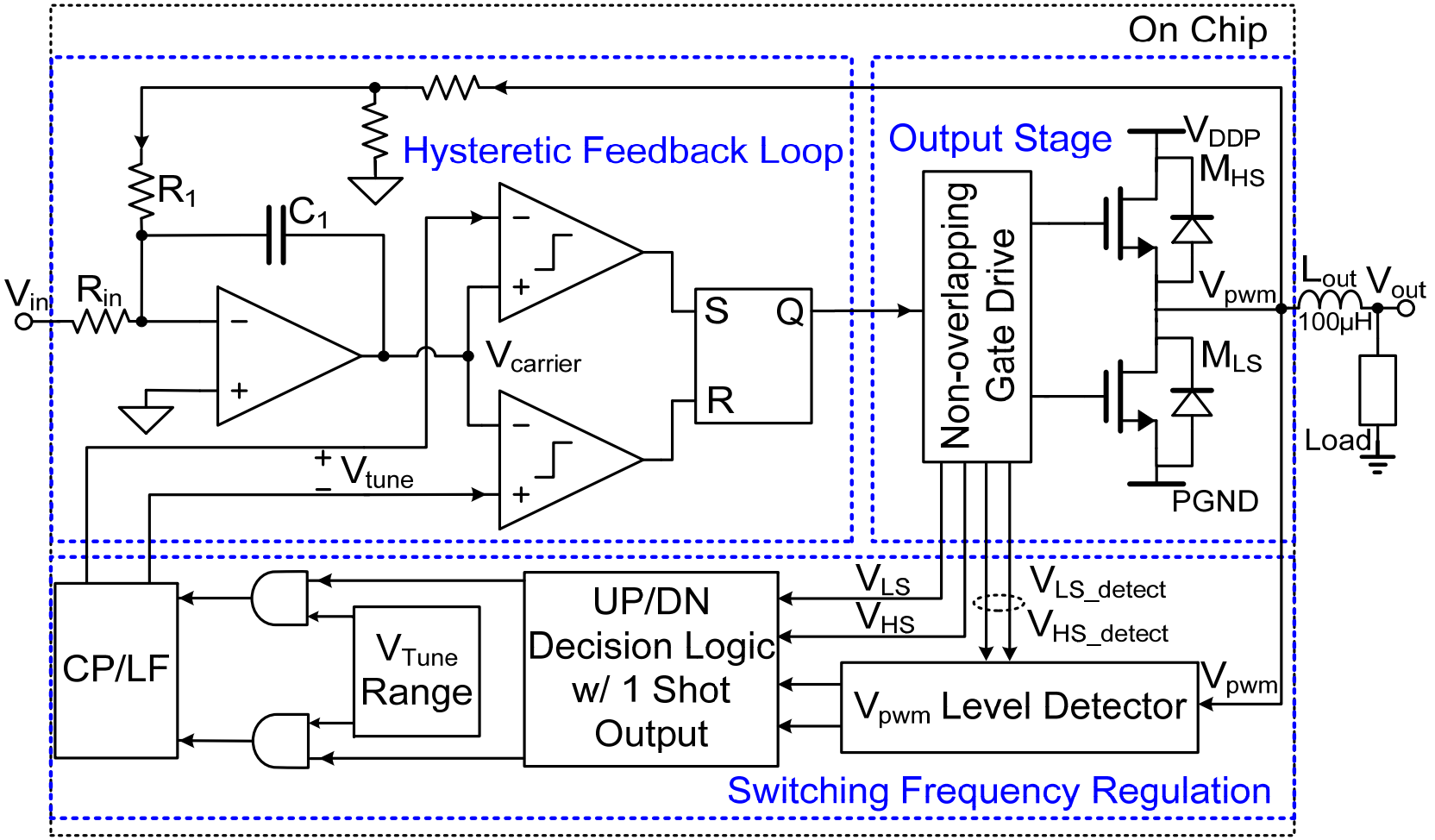


Outline

- Introduction
- Power Dissipation in Class-D Output Stages
- Switching Frequency Regulation for Optimal Efficiency
- Circuit Implementation
- Measurements
- Conclusion

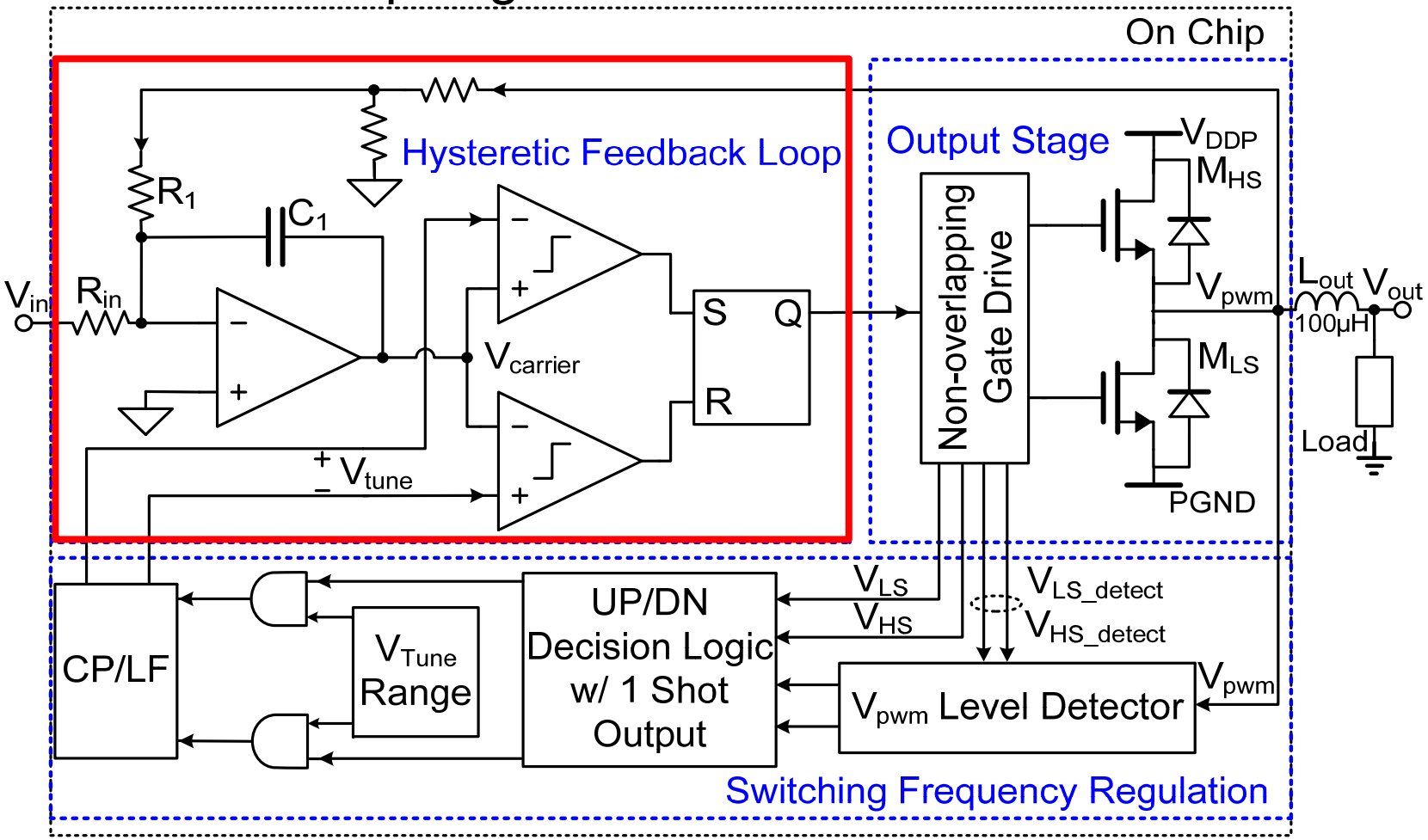
Overview of Topology

- Switching frequency regulation added to a 1st-order hysteresis-based class-D amplifier



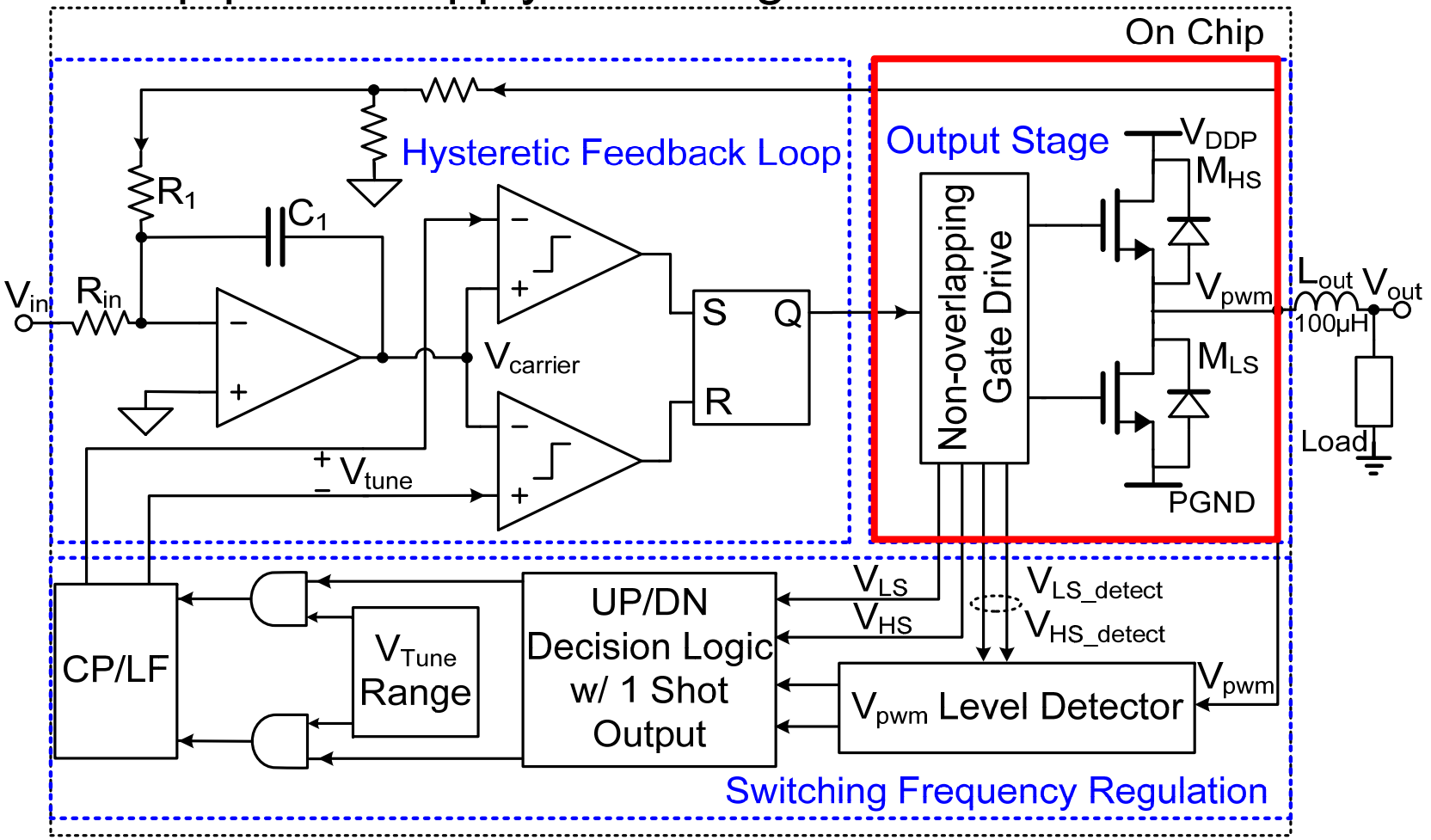
Hysteretic Feedback Loop

- Sufficient loop gain
- Fixed-carrier topologies also feasible



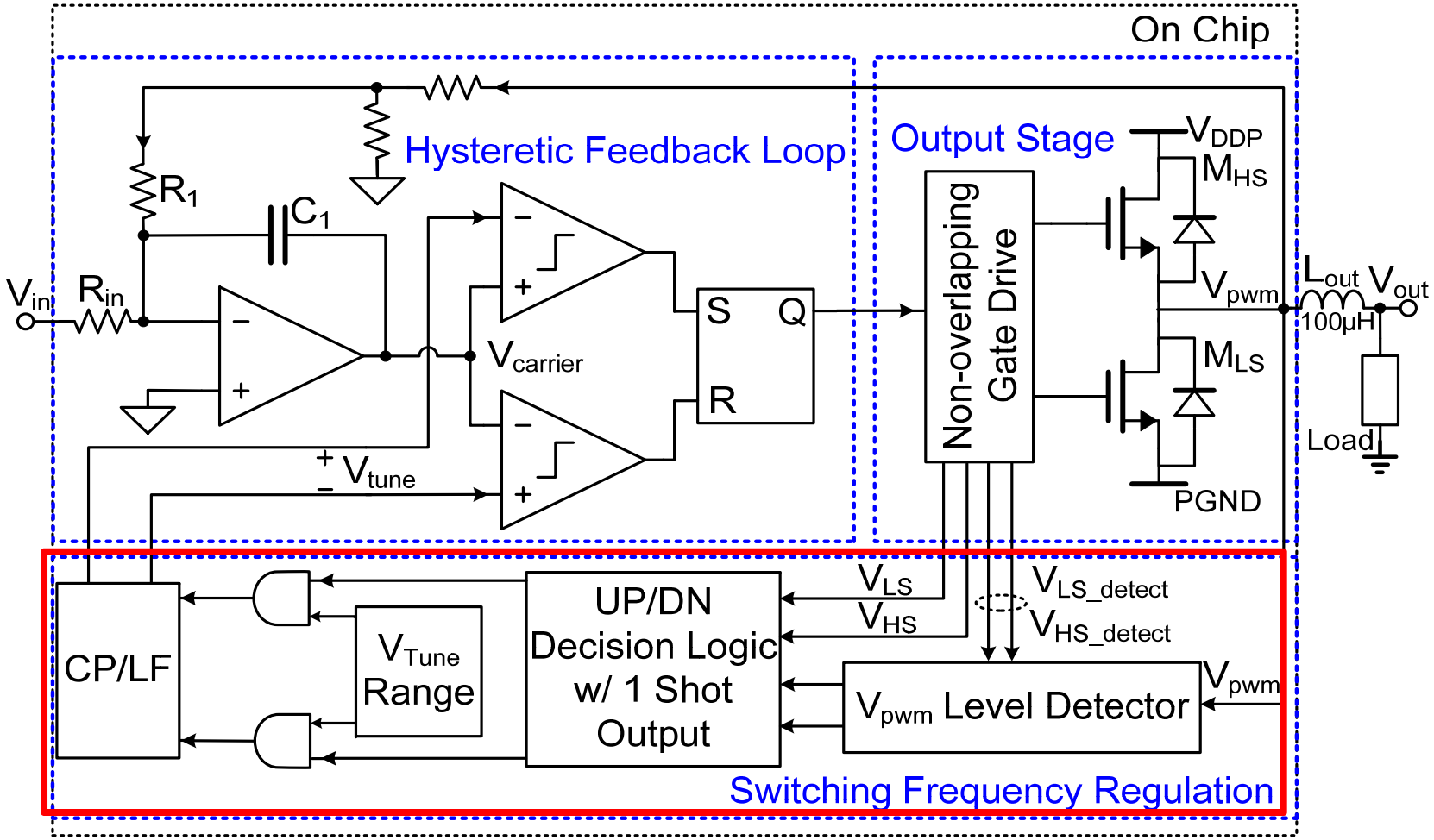
80V Output Stage

- DMOS devices with 80V V_{ds} and 3.3V V_{gs}
- On-chip power supply bouncing issue

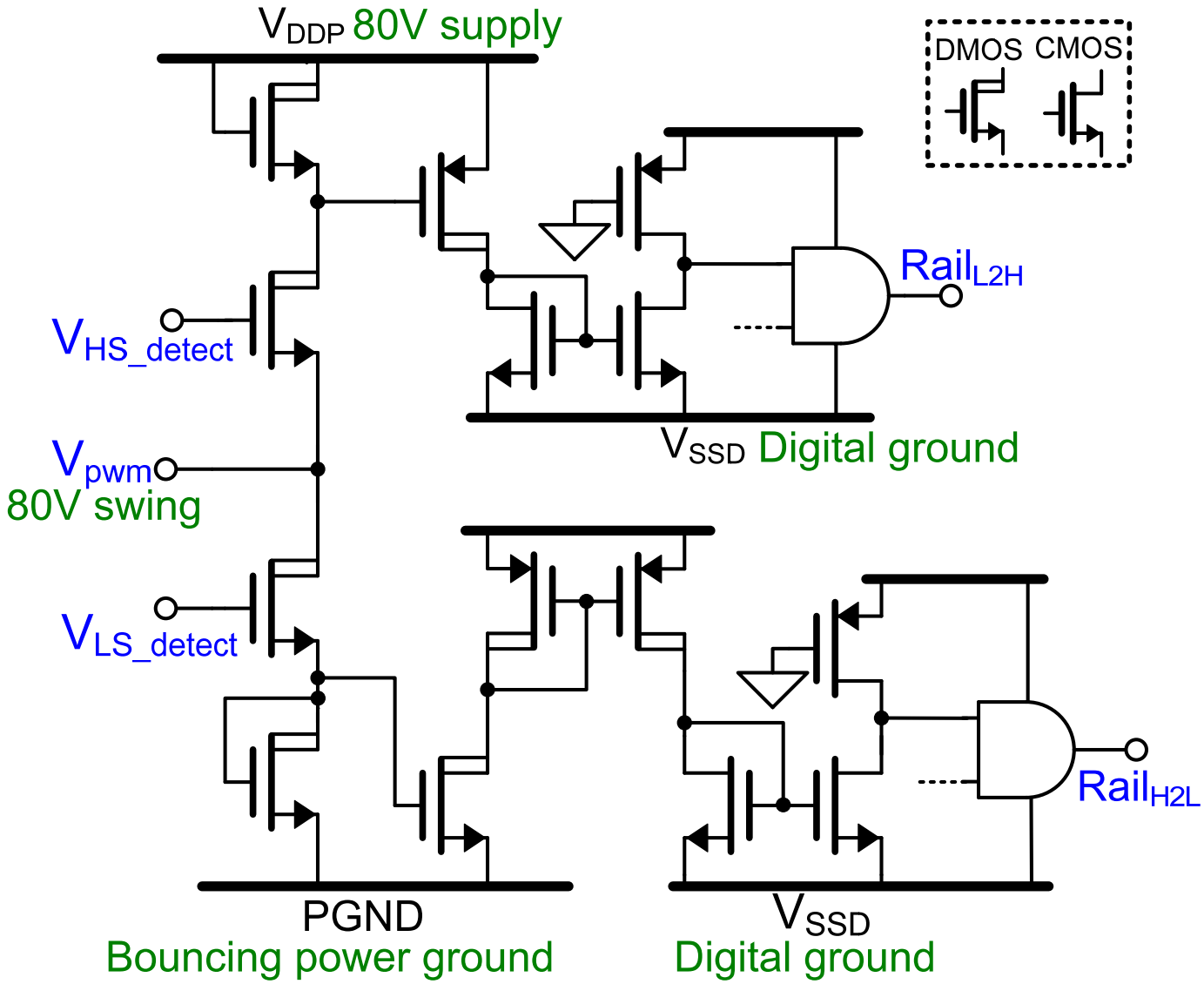


Switching Frequency Regulation

- Generating V_{tune} based on V_{LS}-V_{pwm}, V_{HS}-V_{pwm} timing

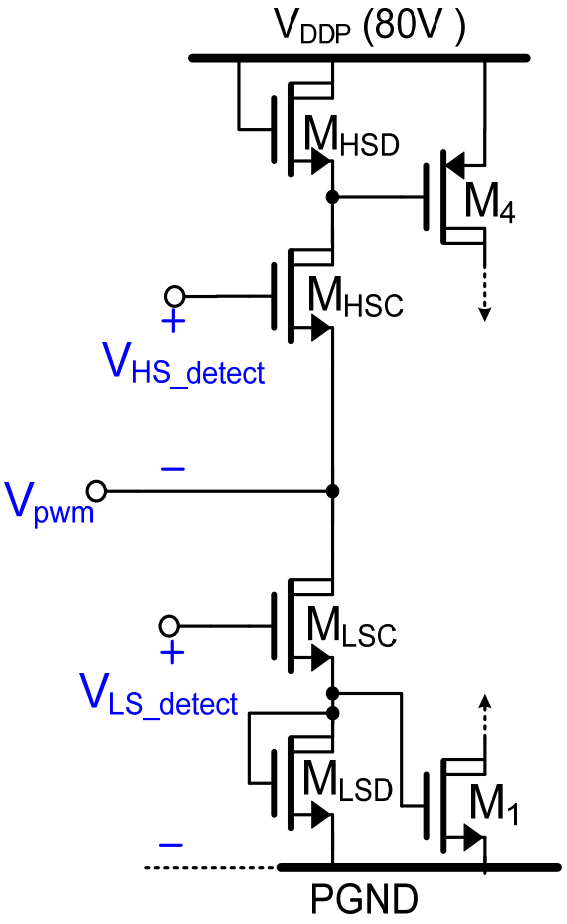


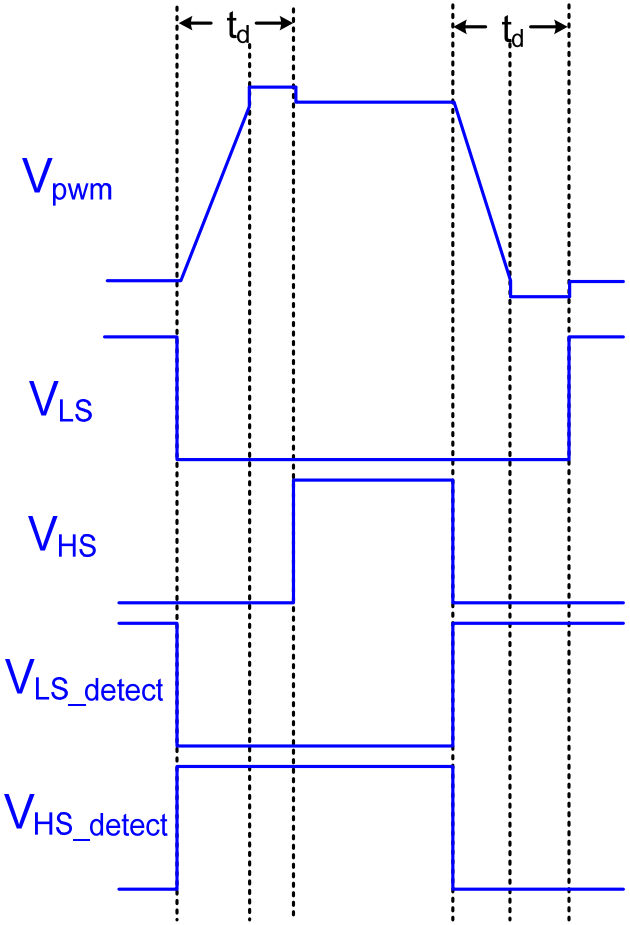
V_{pwm} Level Detector



Level Detection

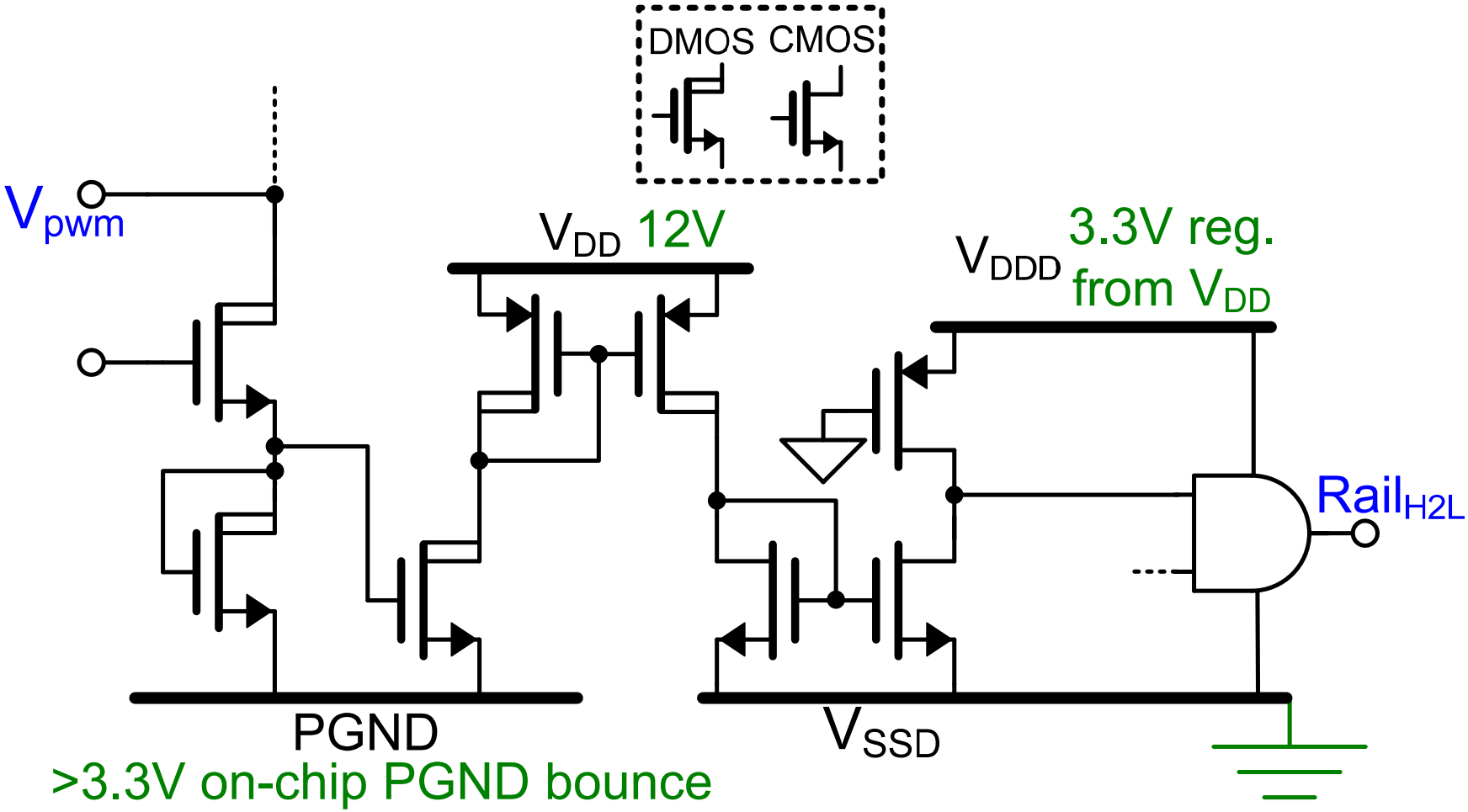
- Avoid DC current from 80V
- $M_{HSC(LSC)}$ divides the 80V V_{pwm} swing.





Level Shifting Referring to V_{SSD}

- >3.3V on-chip supply bounce ➔ two step level shift

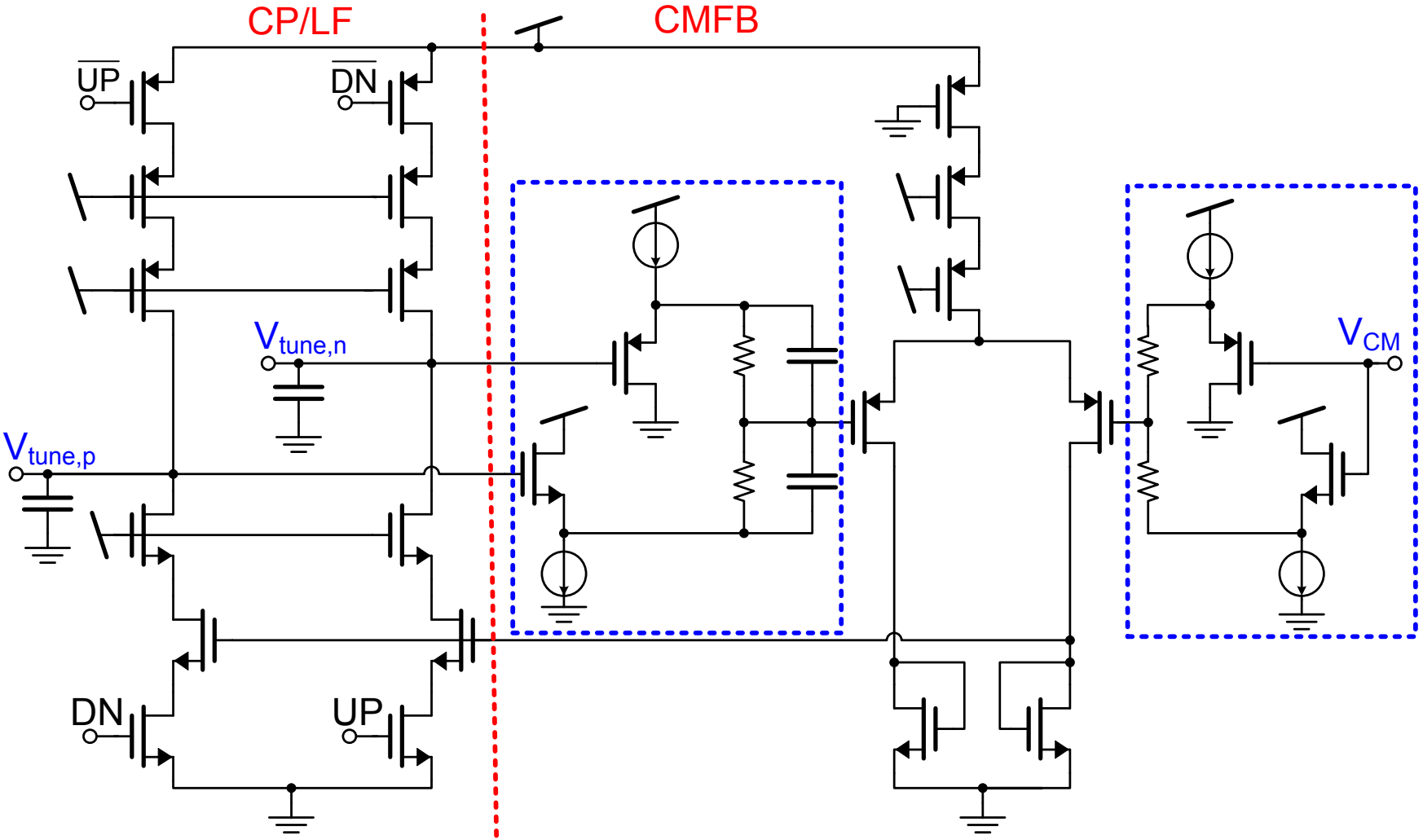


UP/DN Decision Logic

- *Both* V_{pwm} levels already at the other supply rail @ V_{LS} (V_{HS}) rising edge ➔ *Increase* f_{sw}
- *Either* V_{pwm} level not yet reached the other supply rail @ V_{LS} (V_{HS}) rising edge ➔ *Decrease* f_{sw}

Charge Pump/Loop Filter

- $V_{tune,p(n)}$: high impedance & can reach the supply rail

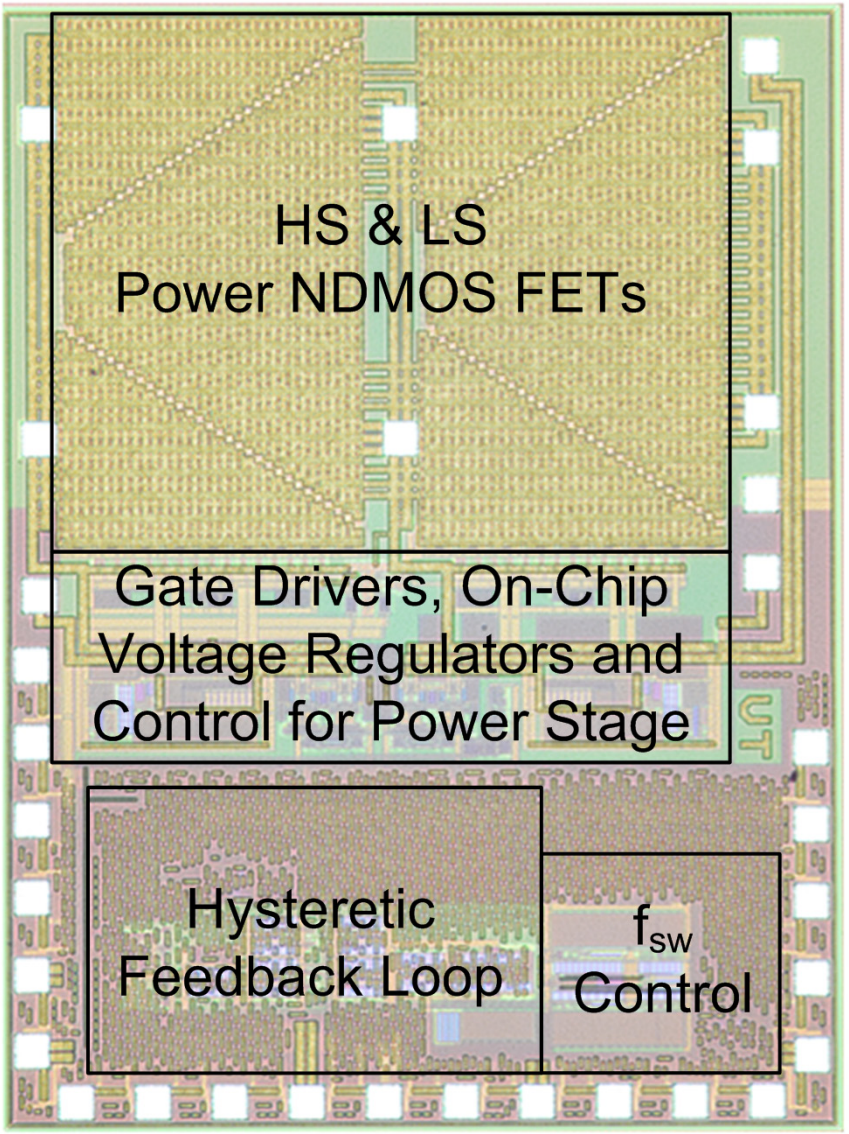


Outline

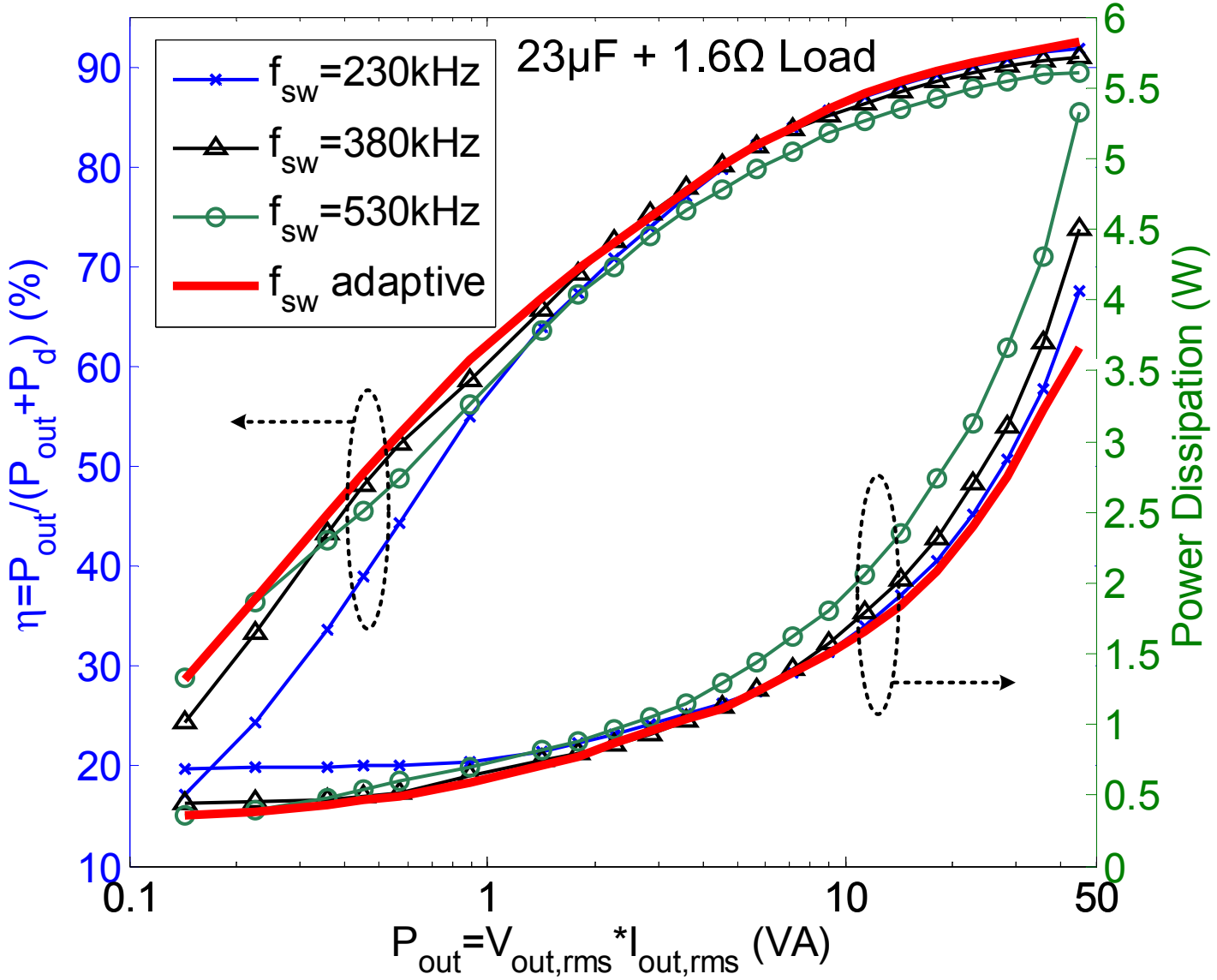
- Introduction
- Power Dissipation in Class-D Output Stages
- Switching Frequency Regulation for Optimal Efficiency
- Circuit Implementation
- Measurements
- Conclusion

Chip Photograph

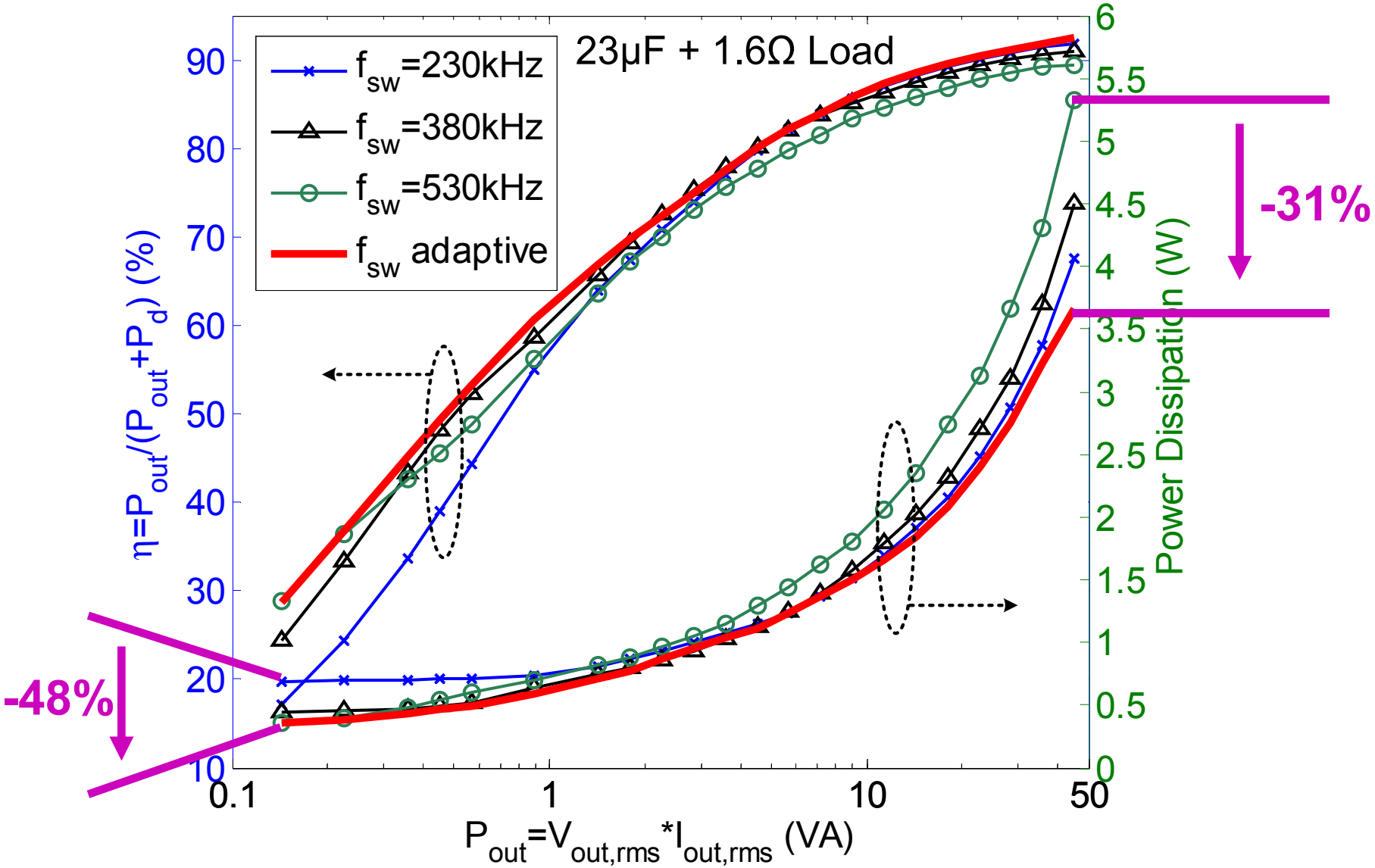
- 0.14μm SOI BCD technology
- 3.4mm*2.5mm



Power Efficiency Measurements



Power Efficiency Measurements



Performance Summary

Parameters	This work		[2]	[3]	[4]	[5]
Type	Piezo Driver		Audio Amp.	Audio Amp.	Audio Amp.	Audio Amp.
V_{DDP}	80V		60V	20V	50V	18V
$P_{out,max}$/Channel	45VA(1)	45W(2)	100W	20W	240W	13W
Efficiency @ $P_{out,max}$	93%	91%	>90%	89%	N/A	88%
Efficiency @ 0.1* $P_{out,max}$	80%	84%	N/A	<75%	N/A	<70%
Efficiency @ 0.01* $P_{out,max}$	49%	51%	N/A	<30%	N/A	<30%
Idle Loss/Channel (w. output filter)	0.36W		1.6W	0.5W	2.1W	N/A
THD+N	0.015% (@9VA, f_{sig}=100Hz) 0.94% (@45VA, f_{sig}=500Hz)		0.017% (@1W, f_{sig}=1kHz)	0.01% (@10W, f_{sig}=1kHz)	<0.1%	0.7% (@13W, f_{sig}=1kHz)

(1) Load = 23μF+1.6Ω in series

(2) Load = 12Ω

Outline

- Introduction
- Power Dissipation in Class-D Output Stages
- Switching Frequency Regulation for Optimal Efficiency
- Circuit Implementation
- Measurements
- Conclusion

Conclusions

- Dominating loss mechanisms in class-D depend on both output power and switching frequency.
- V_{pwm}-level-based switching frequency regulation ensures optimal efficiency for all output powers.
- A class-D amplifier simultaneously achieving both high peak efficiency and low idle loss is designed.

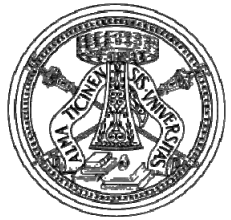
Acknowledgements

- This research is supported by the Dutch Technology Foundation STW.
- We thank NXP for silicon donation.

A 0.0013mm^2 3.6µW Nested-Current-Mirror Single-Stage Amplifier Driving 0.15-to-15nF Capacitive Load with >62° Phase Margin

Zushu Yan [1], Pui-In Mak [1,2], Man-Kay Law [1,2],
Rui P. Martins [1,2,3] and Franco Maloberti [4]

1 – State-Key Laboratory of Analog and Mixed-Signal VLSI
University of Macau, Macao SAR, China
2 – UMTEC, Macao, China
3 – with Instituto Superior Técnico, U of Lisbon, Portugal
4 – University of Pavia, Pavia, Italy



ISSCC 2014

Outline

- **Motivation**
- **Proposed nested current-mirror (NCM) single-stage amplifier**
- **A 4-step NCM amplifier**
- **Experimental results**
- **Comparison with the state-of-the-art**

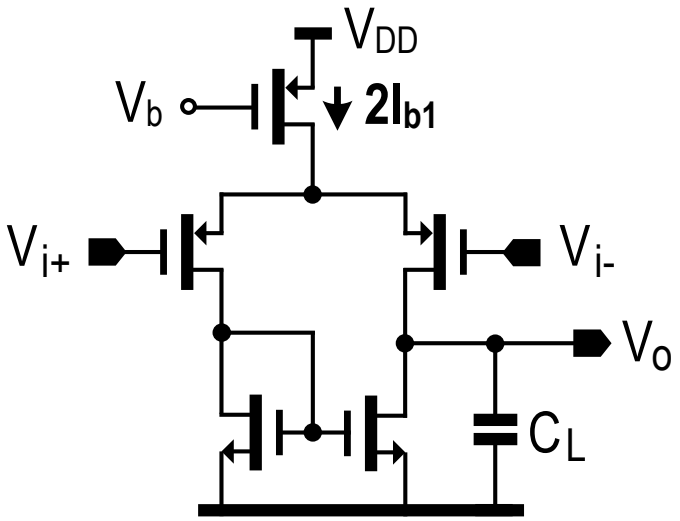
Motivation (1)

- **Multi-stage amplifier**
  - ☑ DC gain ☑ GBW ☑ Output swing ☑ Slew rate
  - ☒ Power ☒ Area ☒ Capacitive (C_L) drivability
- **Single-stage amplifier**
  - ☑ Power ☑ Area ☑ C_L drivability
  - Other metrics exhibit tight trade-offs

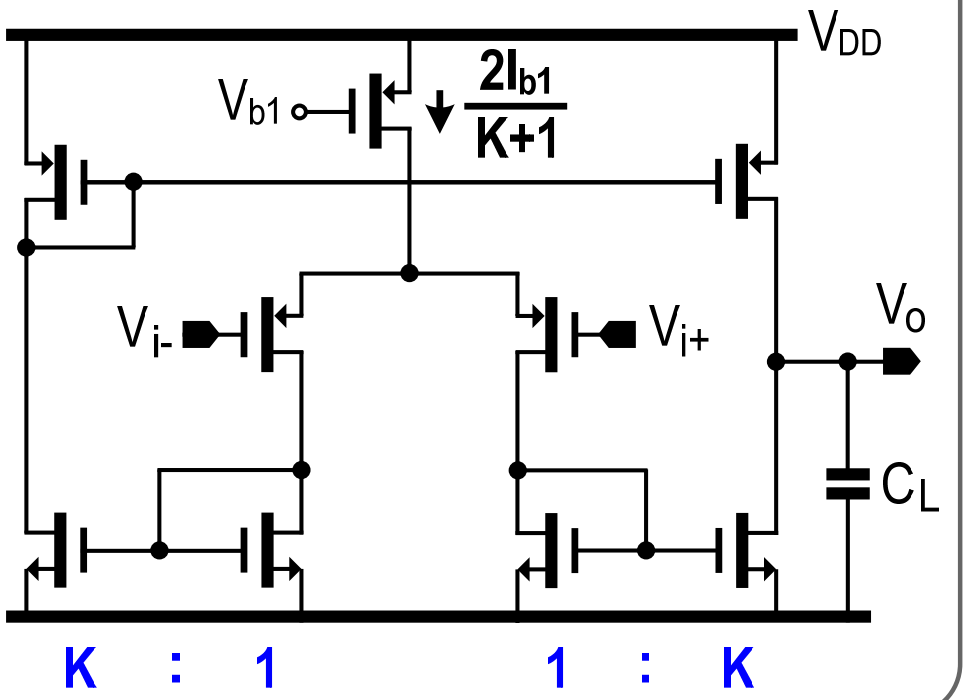
Develop a high-performance buffer amplifier for LCD driver ICs

Motivation (2)

Differential-Pair (DP) Amplifier



Current-Mirror Amplifier



DP Amplifier

☑ Low Noise

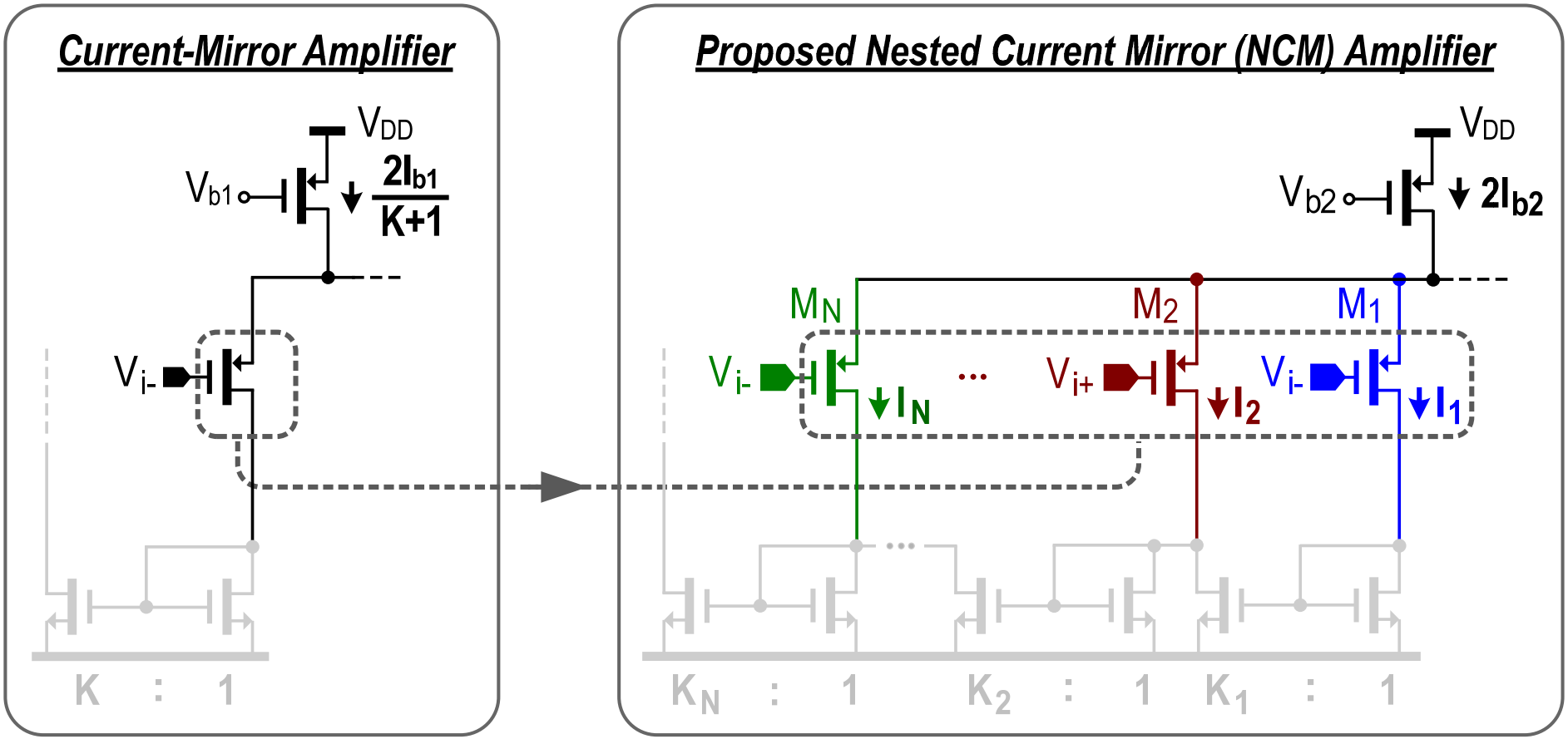
☑ Most power-efficient

Current-mirror amplifier

☑ Wide output swing

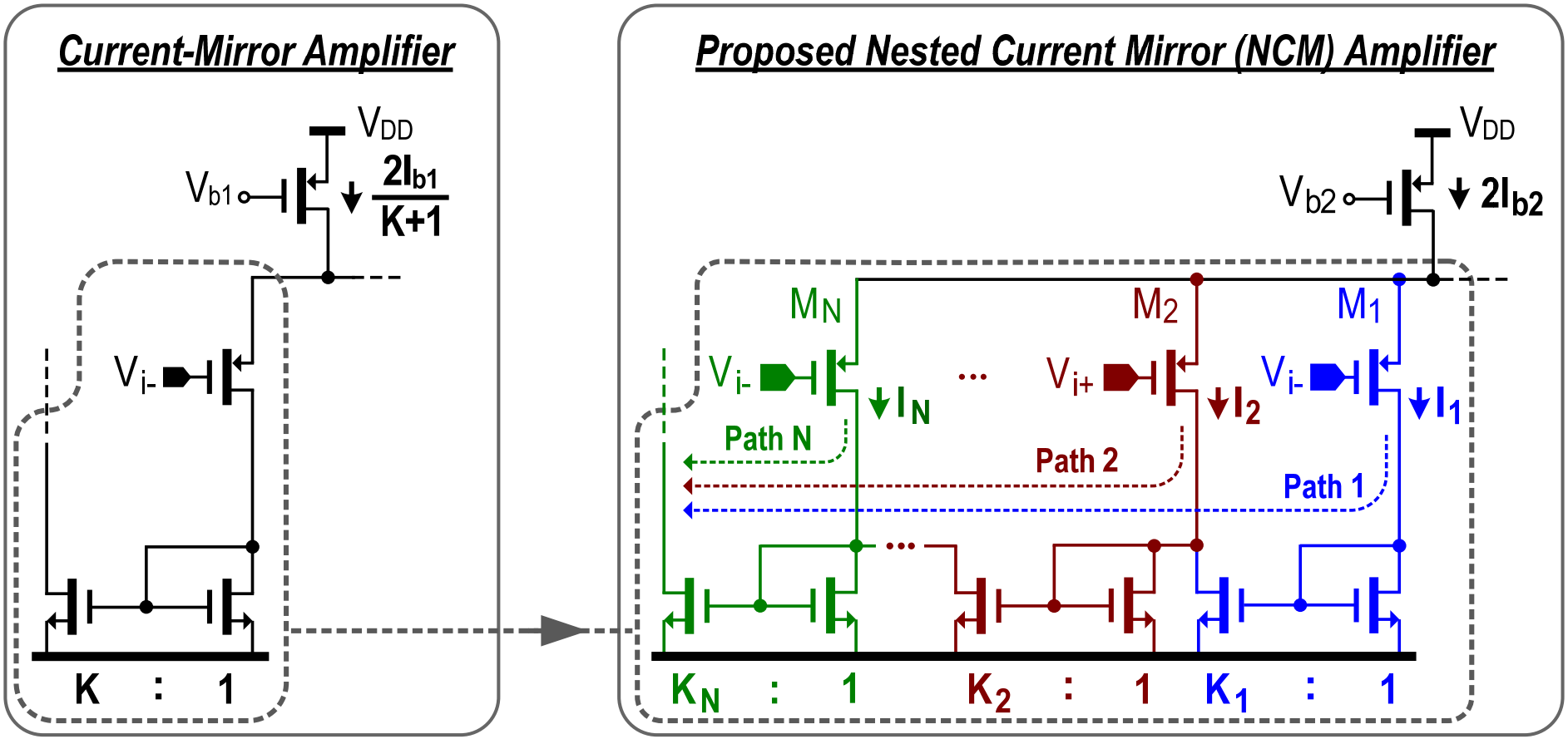
☑ Performance leverage through the mirror ratio K

Principle of the NCM Amplifier (1)



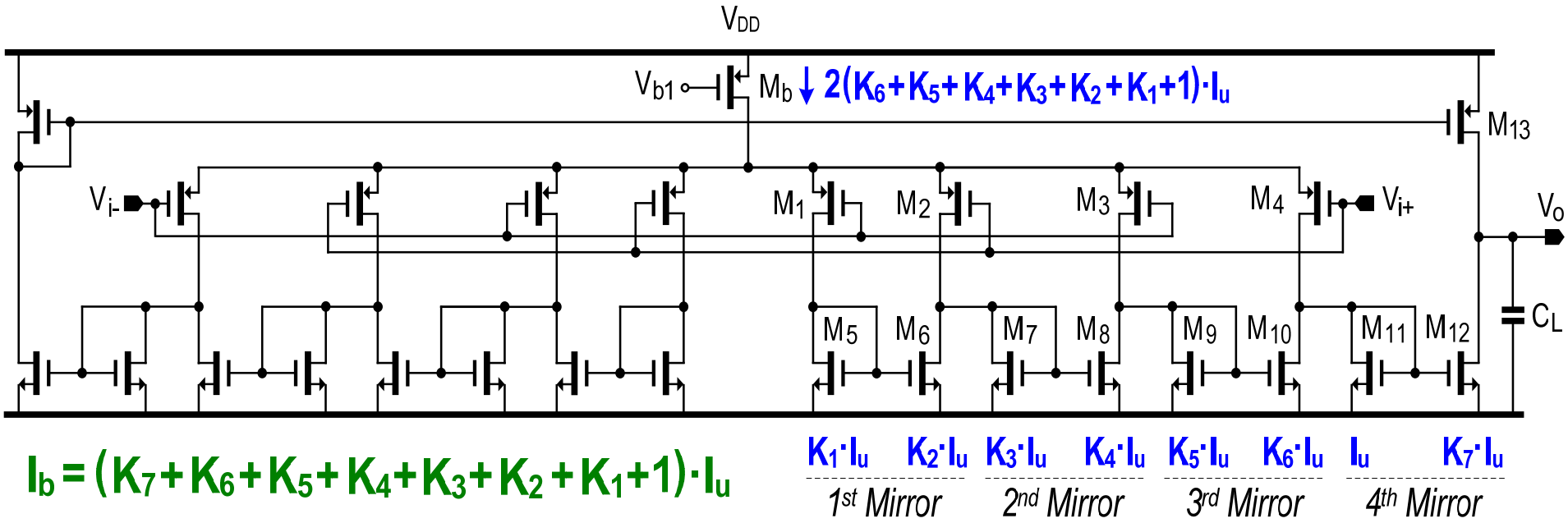
- **Divide the DP transistor into N sub-transistors**
- **Connect their inputs alternatively with V_{i-} and V_{i+}**

Principle of the NCM Amplifier (2)



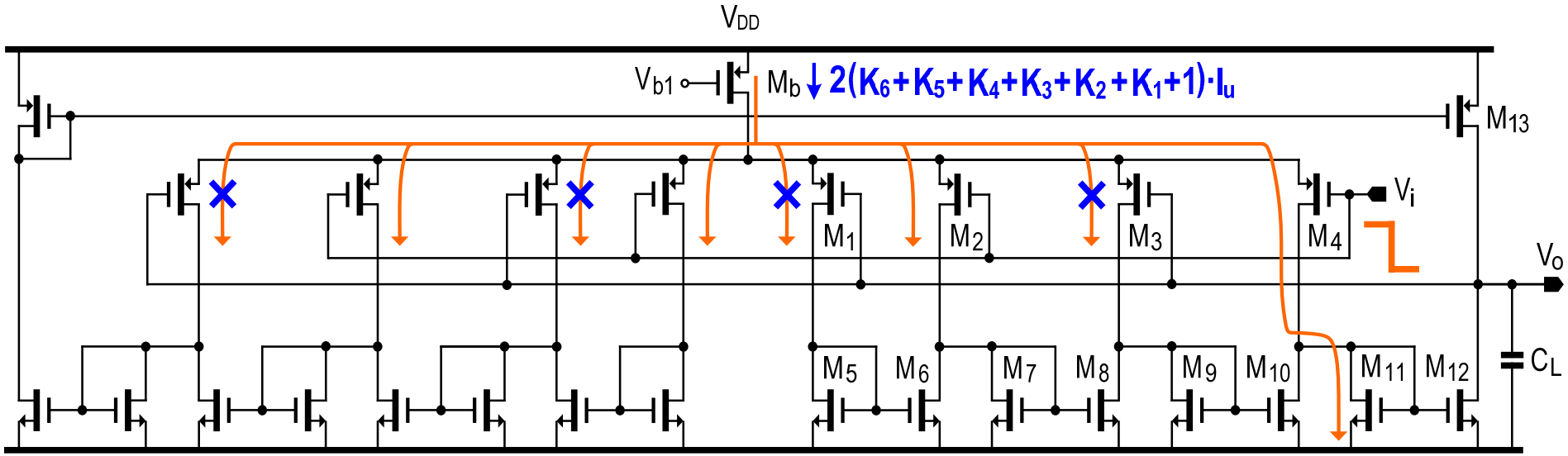
- **Combine the outputs of M_1-M_N through the NCM**
  - ☑ **Concurrently boost $G_{m,eff}$ and R_{out}**
  - ☑ **More design flexibility via K_1 to K_N**

A 4-Step NCM Amplifier



	1st mirror	2nd mirror	3rd mirror	4th mirror
Main concerns	Noise	Gain, GBW	Gain, GBW, SR	SR
Mirror ratio	Smaller	Larger	Larger	Largest
K_1 to K_7	K_1=2, K_2=6	K_3=1, K_4=4	K_5=2, K_6=8	K_7=6

Mirror-Ratio Selection for Slew-Rate (SR)

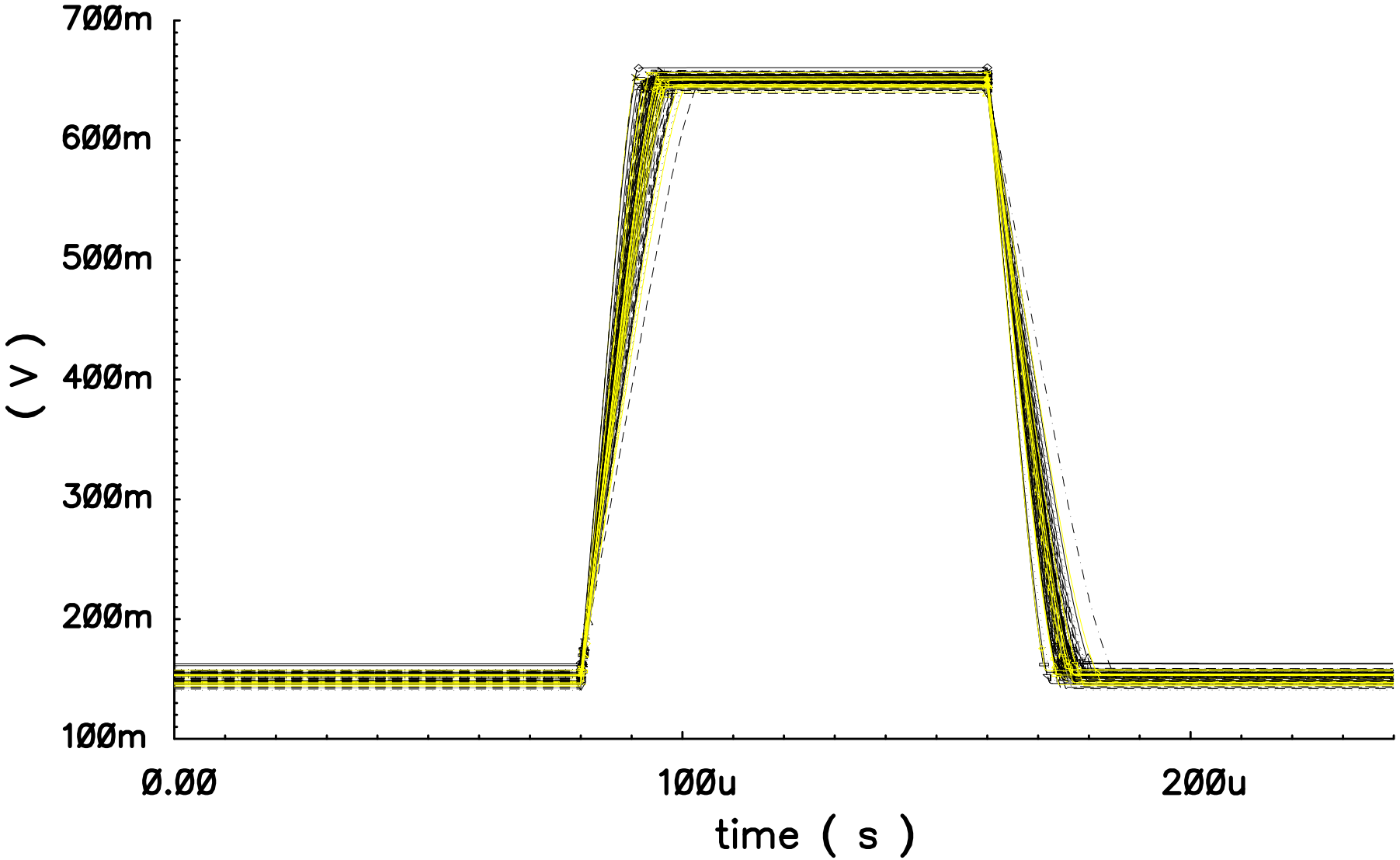


$$I_b = (K_7+K_6+K_5+K_4+K_3+K_2+K_1+1)\cdot I_u$$

$$K_7(K_6+1) > K_7+K_6+K_5+K_4+K_3+K_2+K_1+1$$

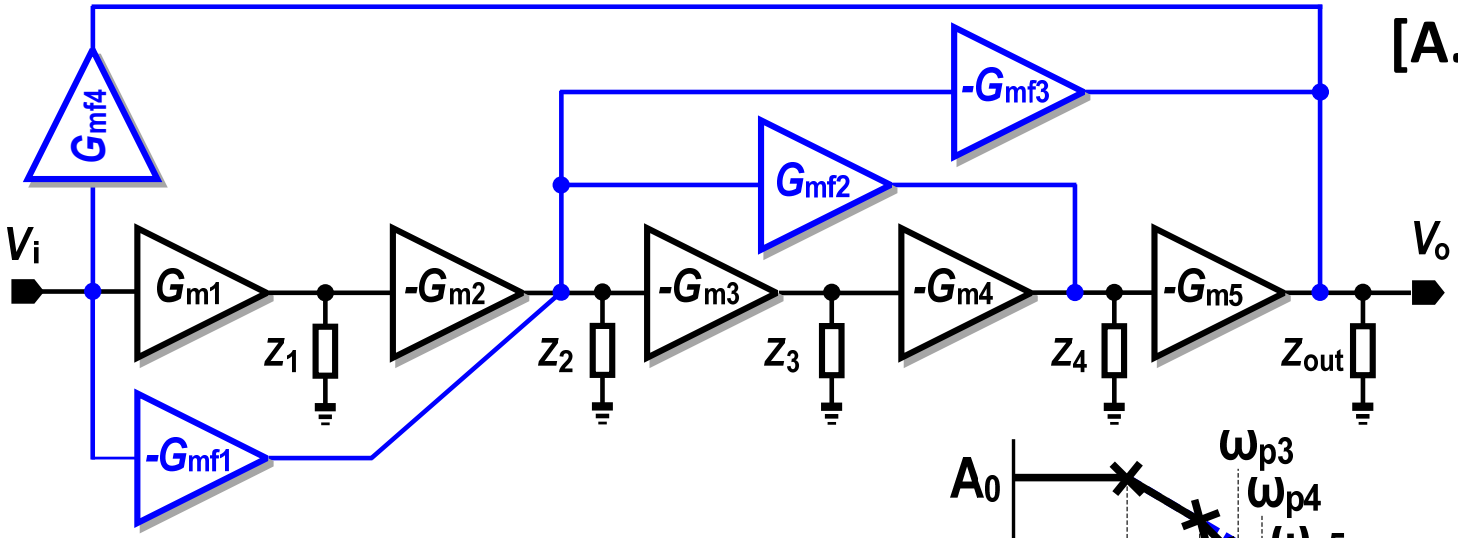
SR of the NCM outperforms the DP

MC-Simulated Large-Step Responses



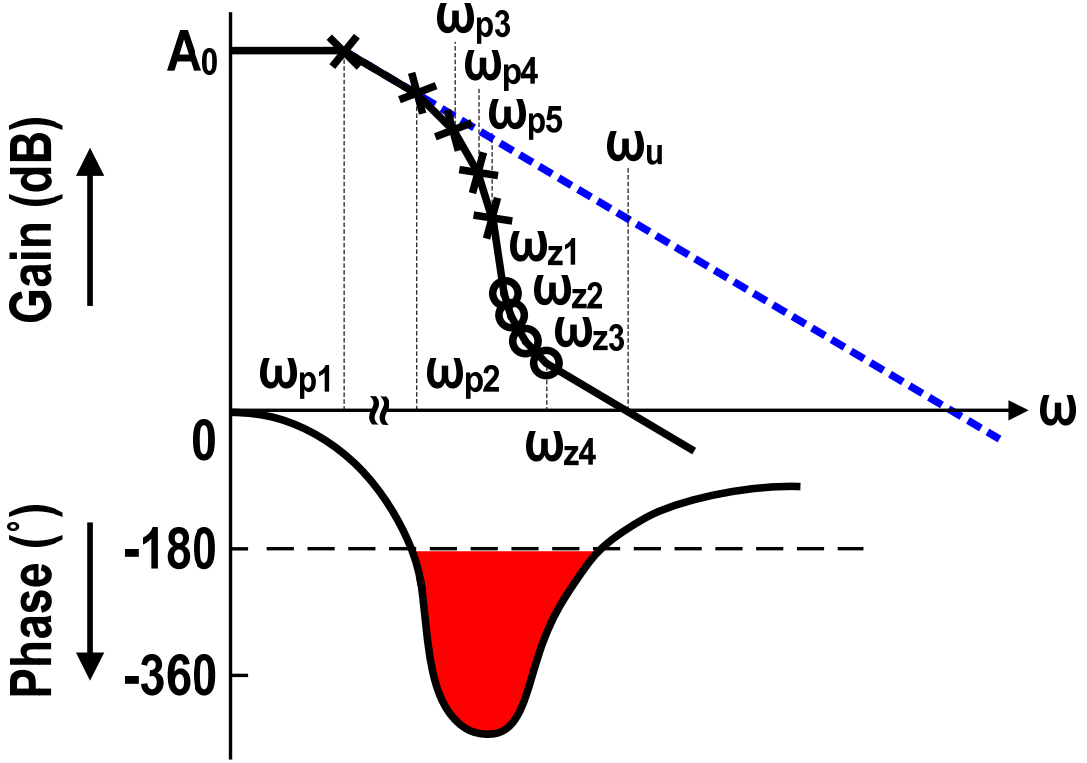
- **Worst 1% T_{S+}: 23 µS and T_{S-}: 25 µS (@0.5V step)**

Stability (1) – Explicit Feedforward Compensation

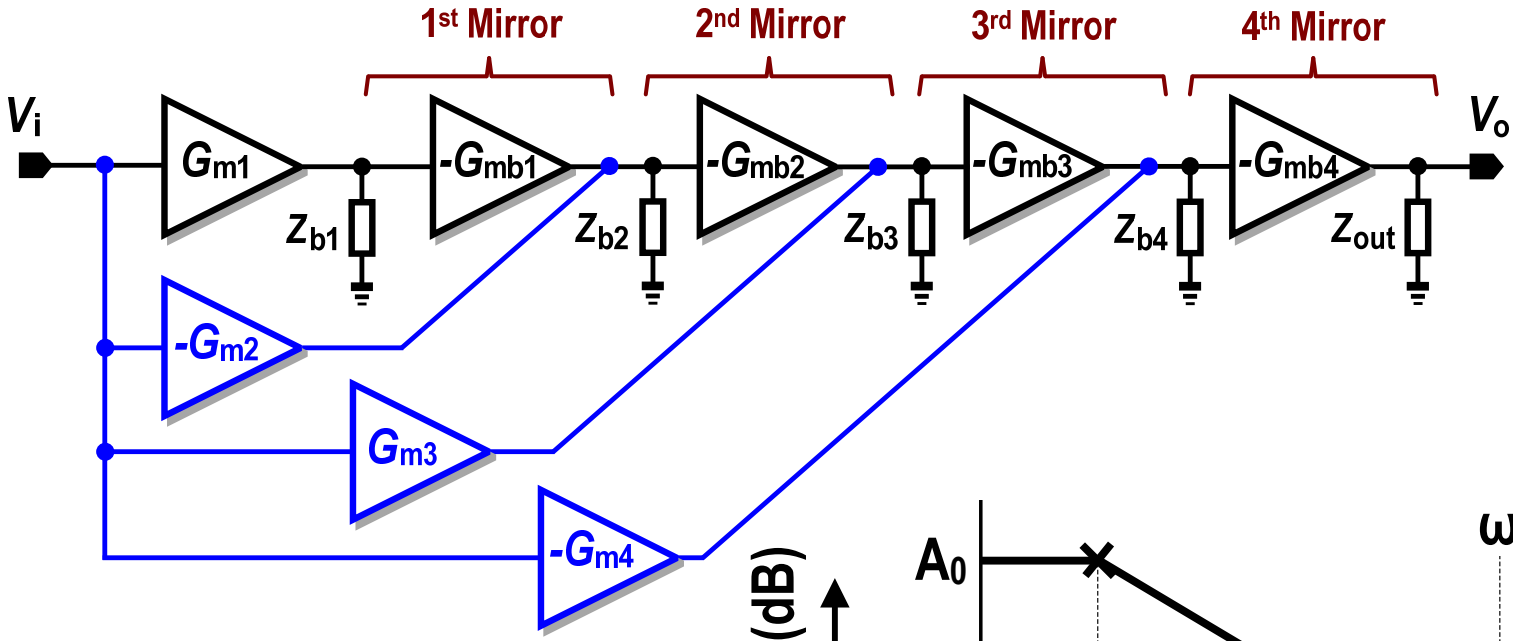


[A. Thomsen, VLSI'98]

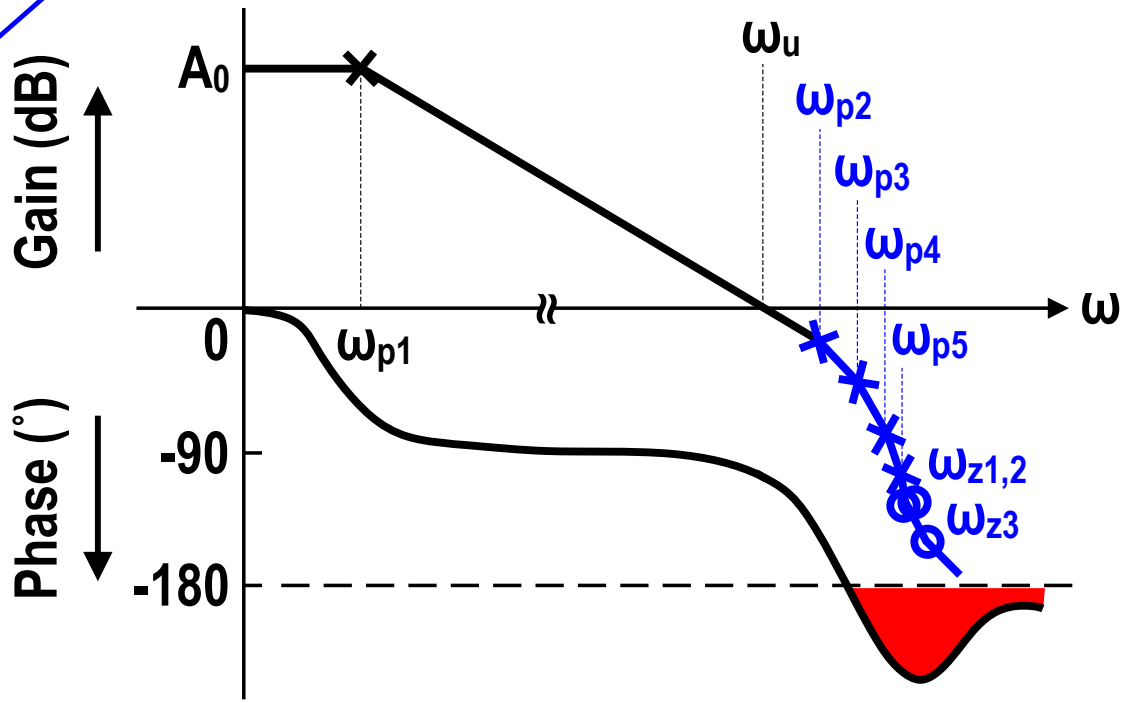
Conditionally-Stable Amplifier:
large-signal stability issue



Stability (2) – Implicit Feedforward Compensation

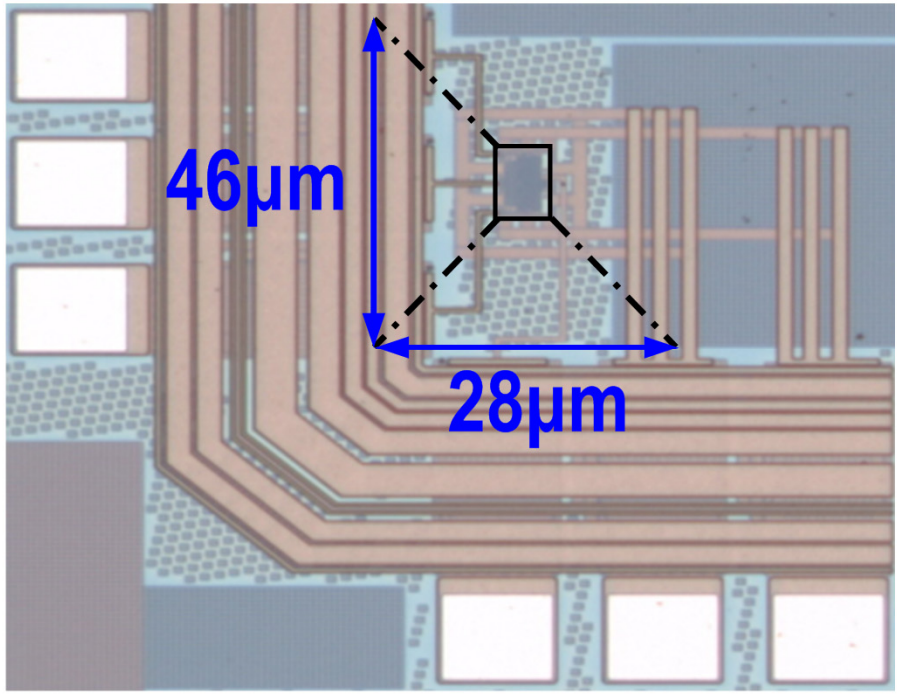


Unconditionally-Stable Amplifier

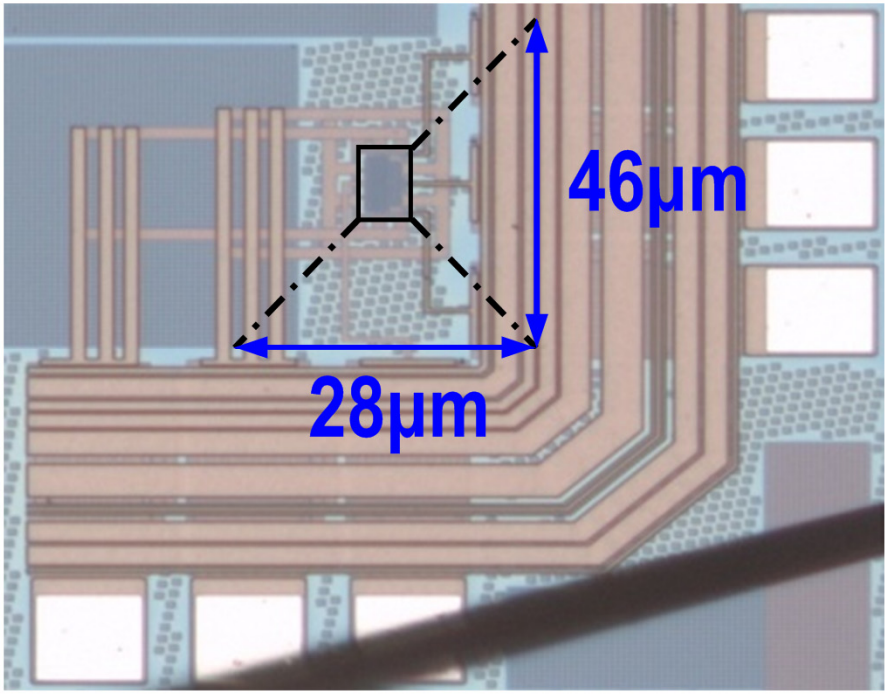


Chip Photos in 0.18µm CMOS

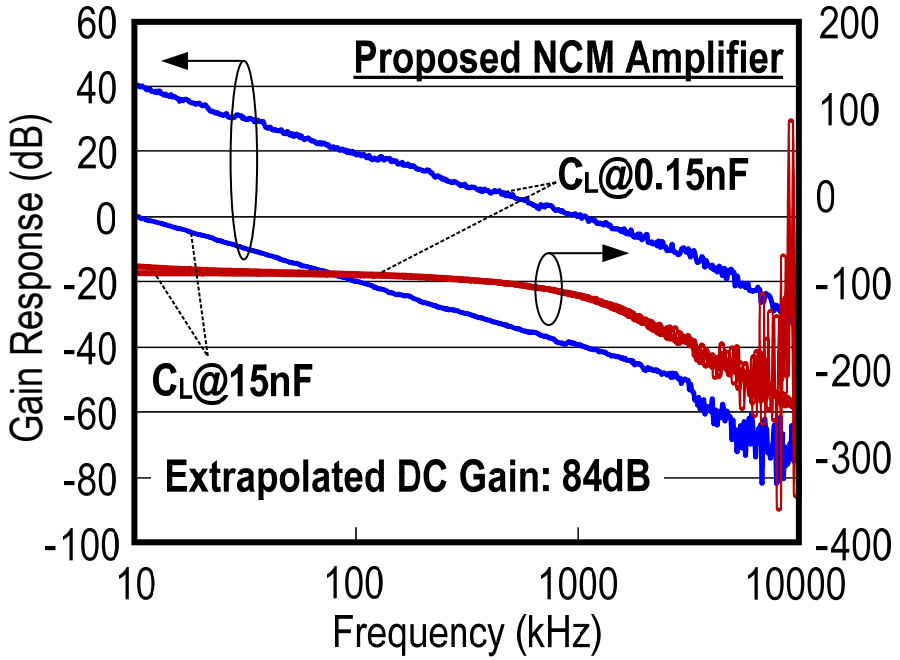
Proposed NCM Amplifier

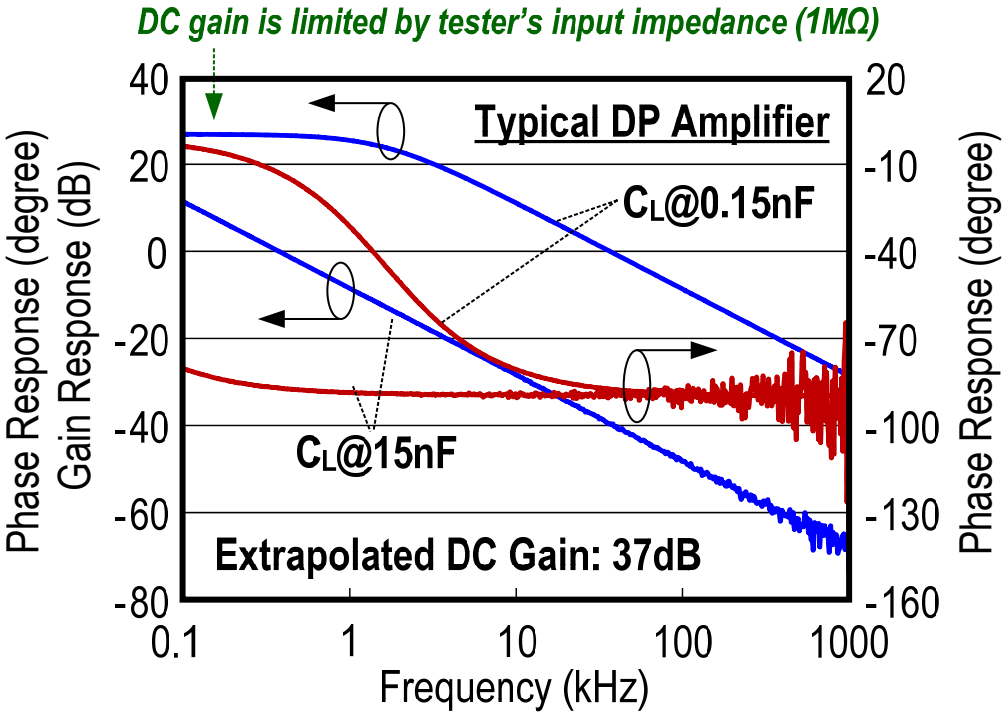


Typical DP Amplifier



AC Responses @ C_L= 0.15 and 15nF



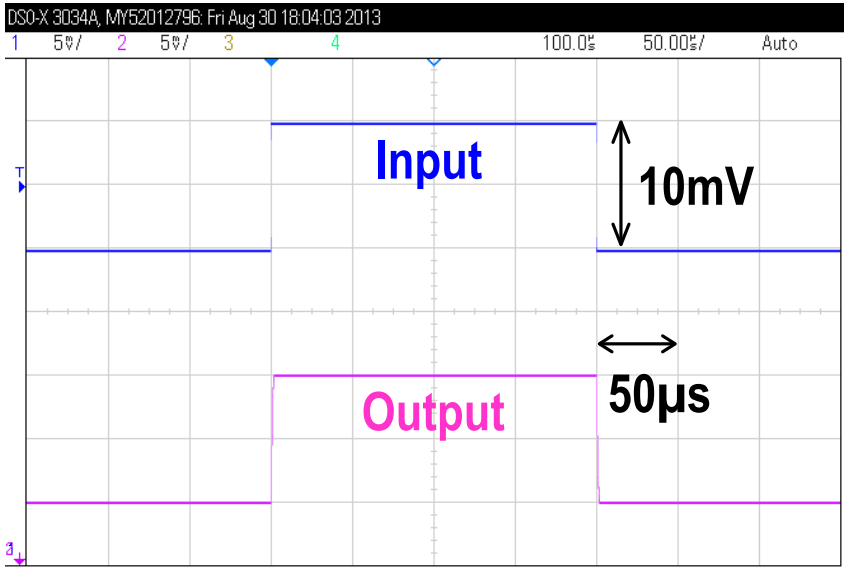


GBW improved by >33x @ C_L ≥0.15nF

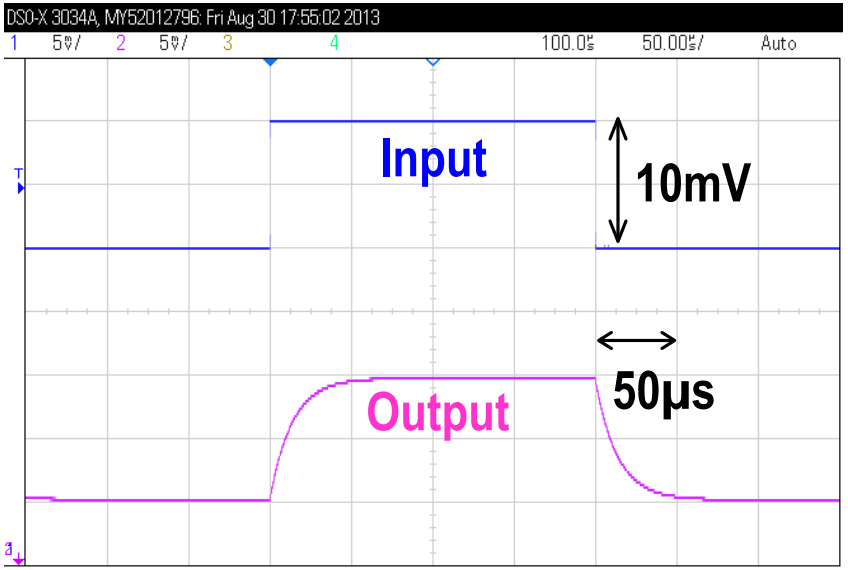
DC Gain enhanced by >40dB @ C_L ≥0.15nF

Small-Step Responses @ C_L = 0.15nF

Proposed NCM Amplifier



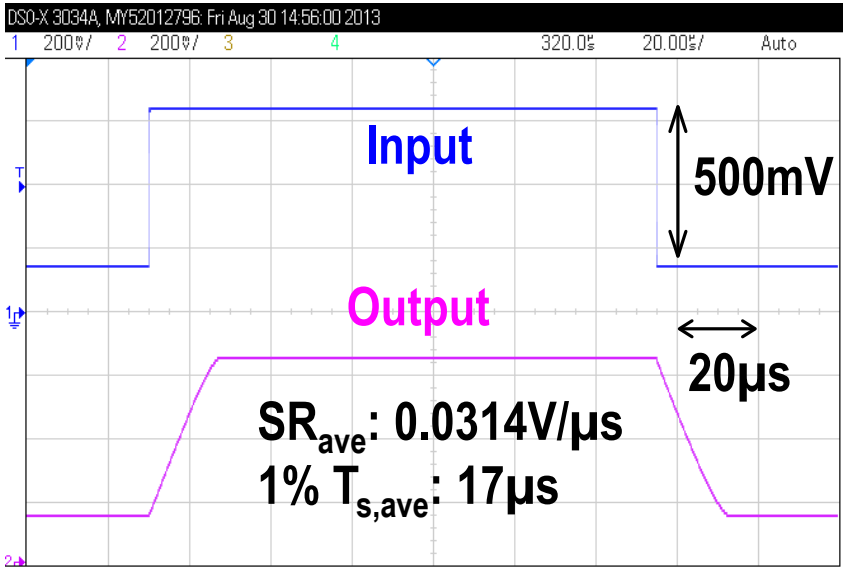
Typical DP Amplifier



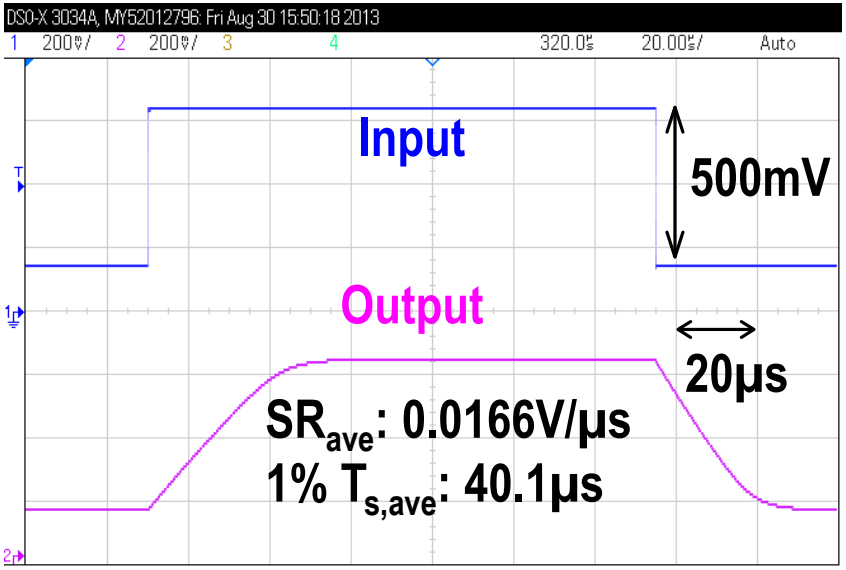
1% T_s Reduced by >50x

Large-Step Responses @ C_L = 0.15nF

Proposed NCM Amplifier



Typical DP Amplifier

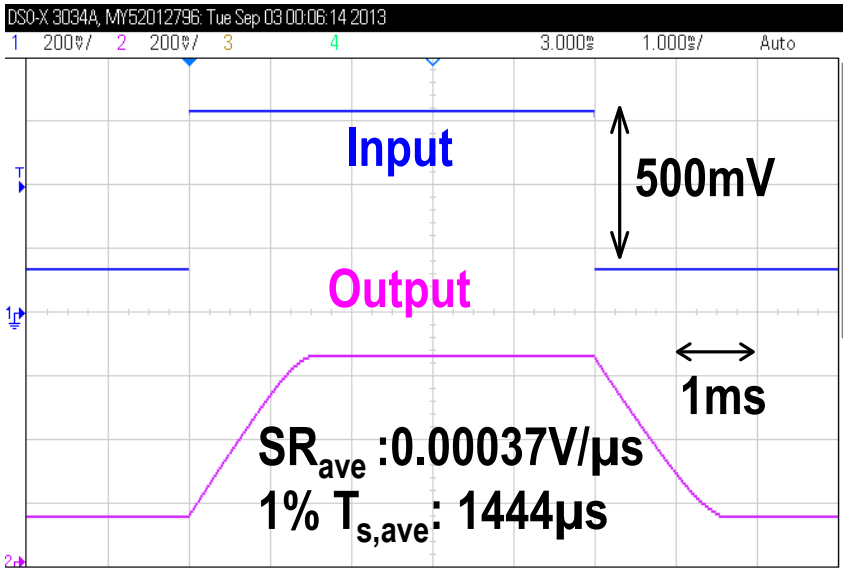


SR_{ave} Improved by >1.8x

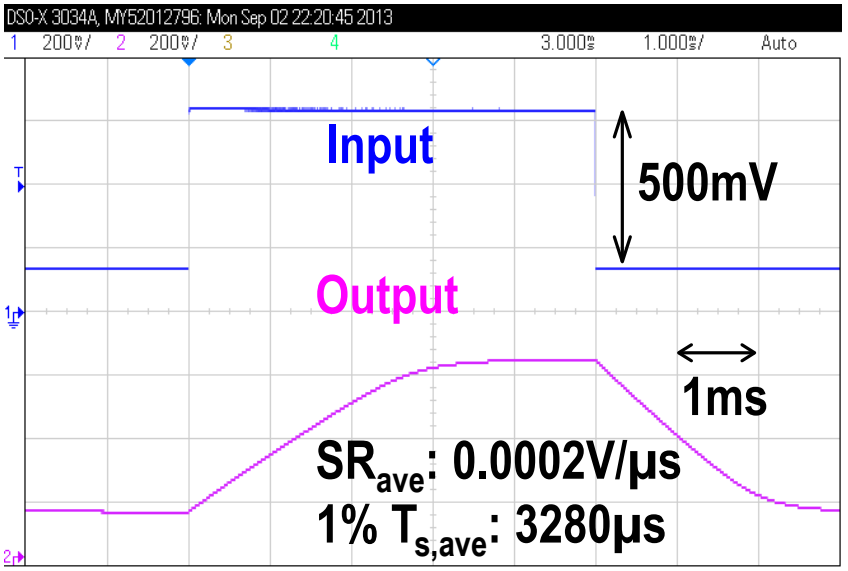
1% $T_{s,ave}$ Reduced by >2.3x

Large-Step Responses @ C_L = 15nF

Proposed NCM Amplifier



Typical DP Amplifier



SR_{ave} Improved by >1.8x

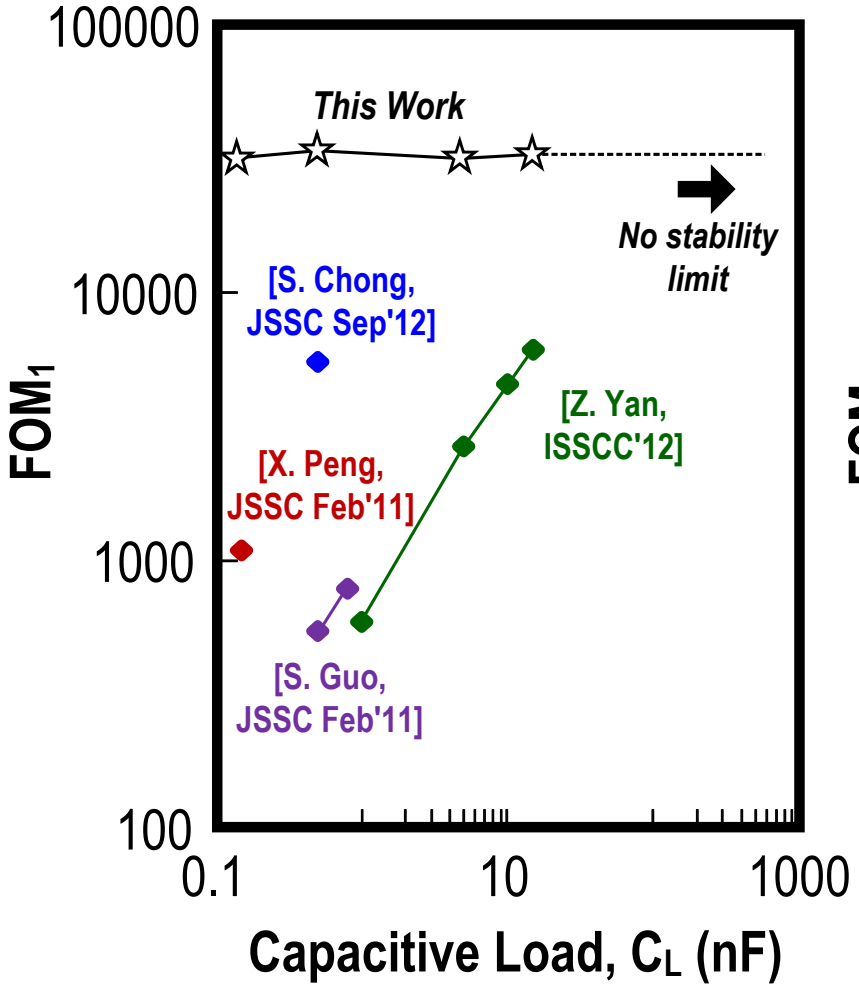
1% $T_{s,ave}$ Reduced by >2.3x

Comparison: NCM vs DP Amplifiers

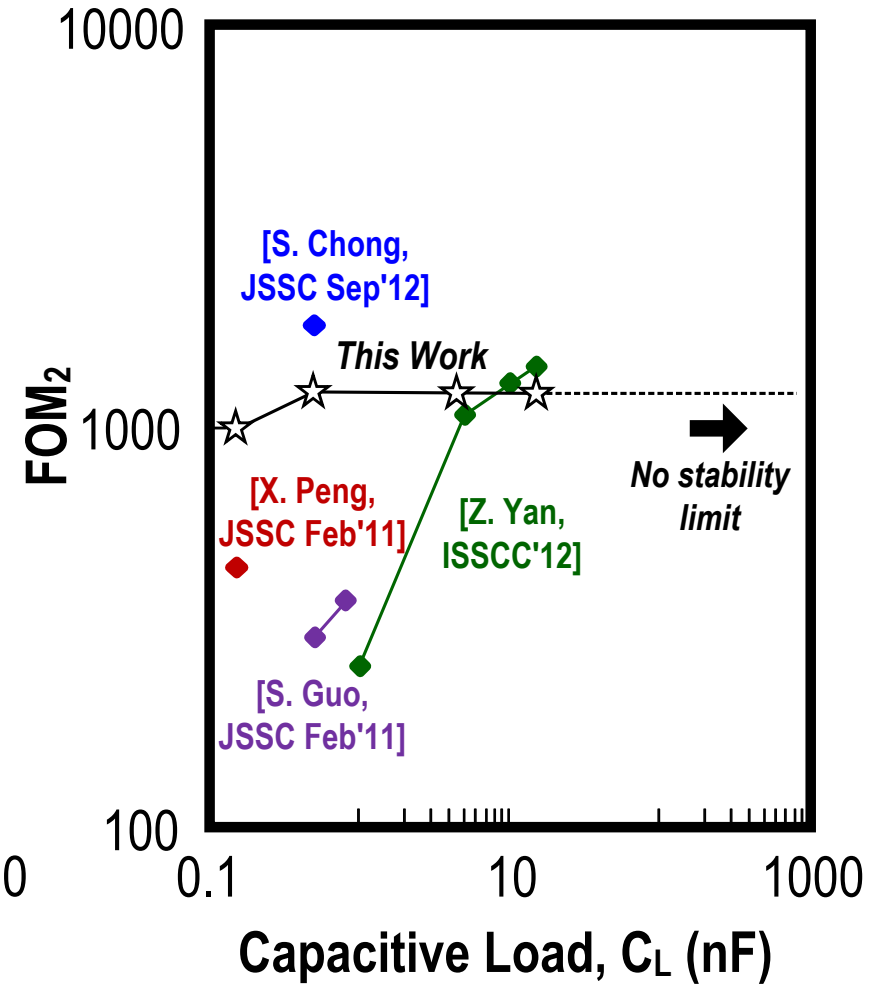
	Proposed NCM Amplifier			Typical DP Amplifier		
Load C_L (nF)	0.15	0.5	15	0.15	0.5	15
GBW (MHz)	1.24	0.396	0.013	0.0371	0.0116	0.00038
Phase Margin (degree)	62.4	81.4	90.2	91.7	92.5	92.9
Gain Margin (dB)	15.9	23.7	56.1	>60	>60	>60
SR_{ave} (V/μs)	0.0314	0.0115	0.00037	0.0166	0.0058	0.0002
1% $T_{s,ave}$ (μs)	17	47.1	1444	40.1	109	3280
DC Gain (dB) (extrapolated)	84			37		
Input-Referred Noise (nV/√Hz)	1470 @ 0.1kHz	440 @ 1kHz	140 @ 10kHz	680 @ 0.1kHz	270 @ 1kHz	106 @ 10kHz
Power (μW) @ V_{DD} (V)	3.6 @ 1.2			3.6 @ 1.2		
Chip Area (mm^2)	0.0013			0.0013		
CMOS Technology	0.18μm			0.18μm		

Comparison with State-of-the-Art

$$FOM_1 = \frac{GBW\ [MHz] \cdot C_L\ [pF]}{Power\ [\mu W] \cdot Area\ [mm^2]}$$



$$FOM_2 = \frac{SR\ [V/\mu s] \cdot C_L\ [pF]}{Power\ [\mu W] \cdot Area\ [mm^2]}$$



Acknowledgments

- **Multi-Year Research Grant of University of Macau**

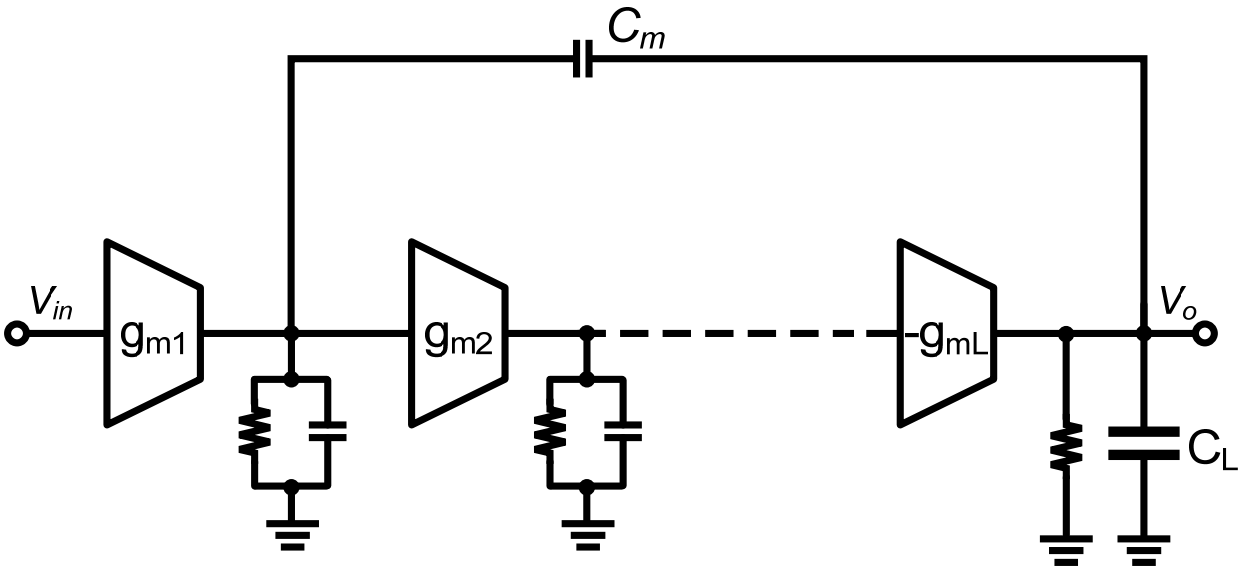
- **Macao Science and Technology Development Fund (FDCT)**

#17.3:
A 0.9V 6.3μW Multistage Amplifier Driving 500pF Capacitive Load with 1.34MHz GBW

Wanyuan Qu, Jong-Pil Im, Hyun-Sik Kim
Gyu-Hyeong Cho
KAIST

Field of Research

Miller-compensated multistage amplifier.

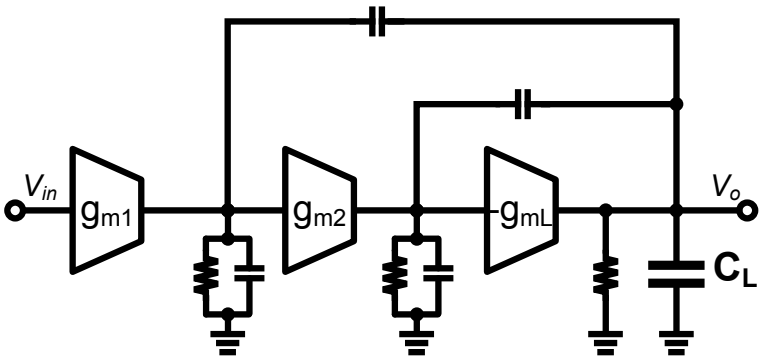


Smaller process requires cascading stages for high gain .

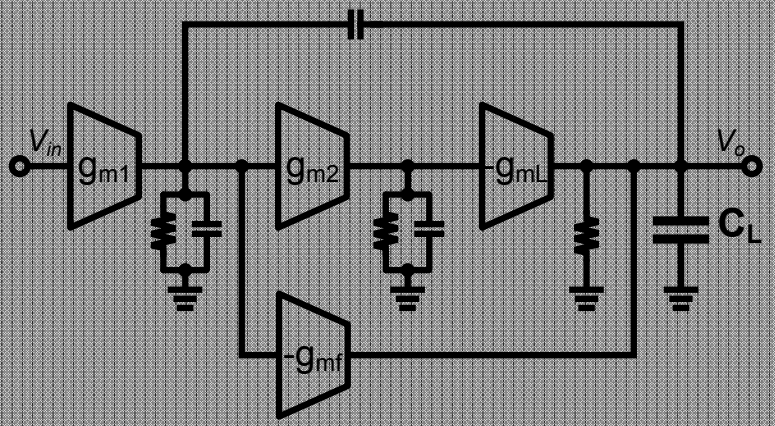
Frequency compensation becomes difficult.

Prior Arts

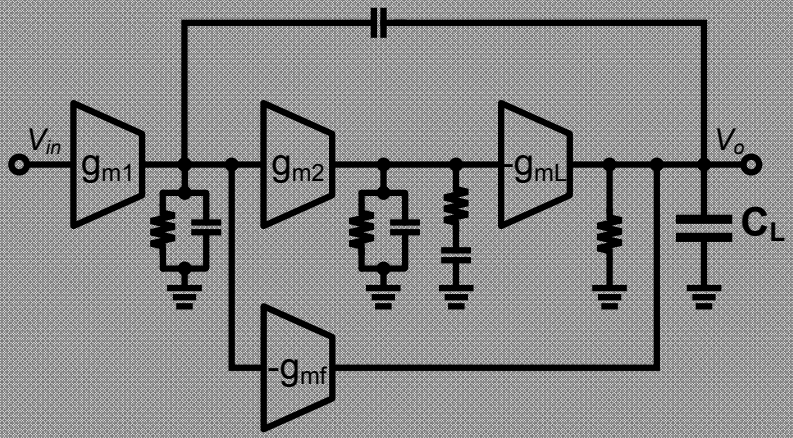
NMC [J. H. Huijsing JSSC 1985]



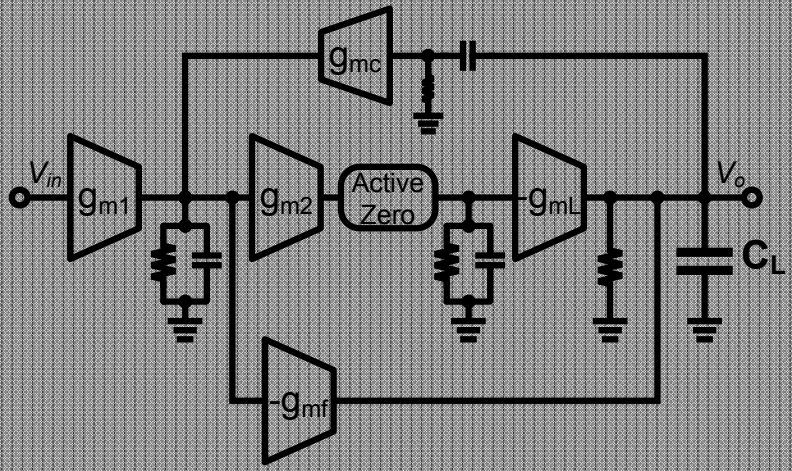
SMFFC [X. Fan JSSC 2005]



IAC [X. Peng JSSC 2011]

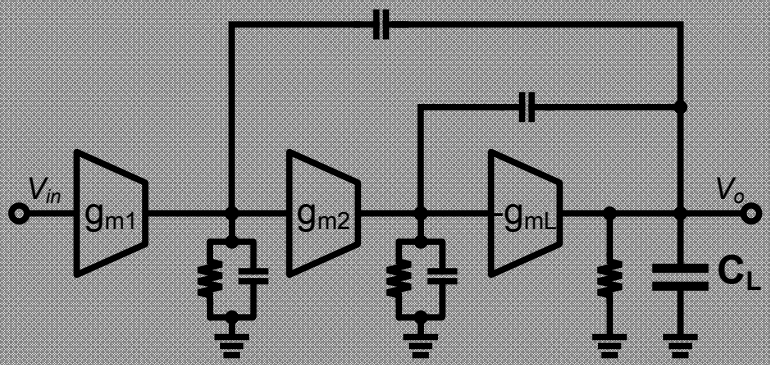


AZC [Z. Yan ISSCC 2012]

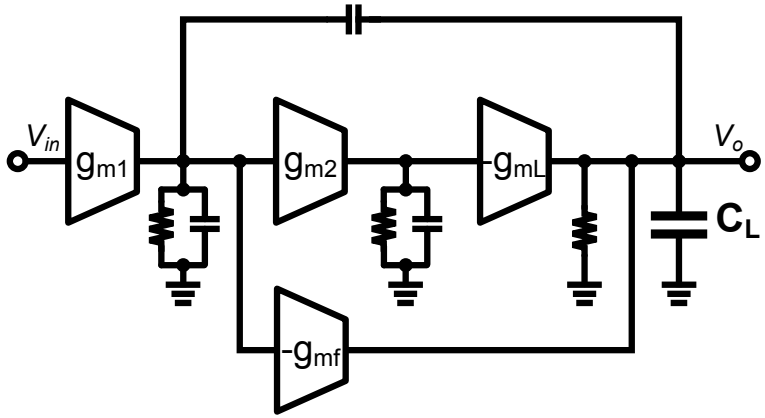


Prior Arts

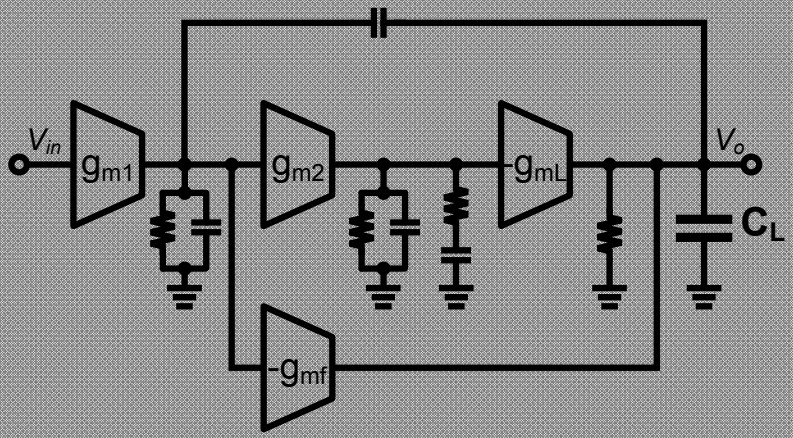
NMC [J. H. Huijsing JSSC 1985]



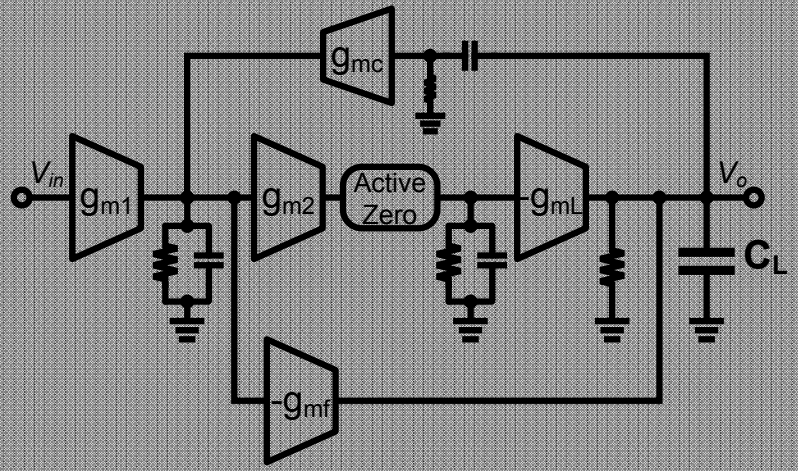
SMFFC [X. Fan JSSC 2005]



IAC [X. Peng JSSC 2011]

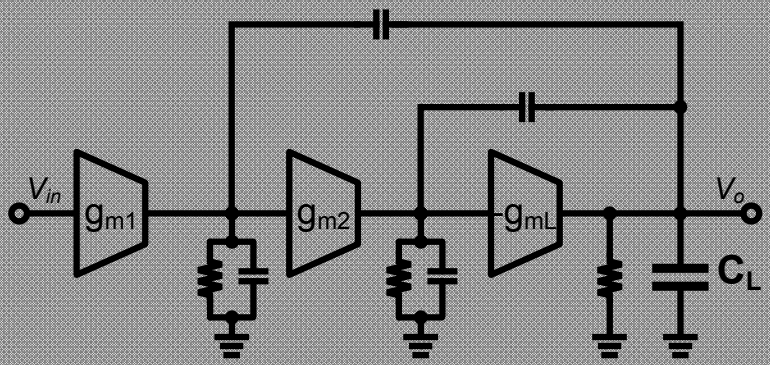


AZC [Z. Yan ISSCC 2012]

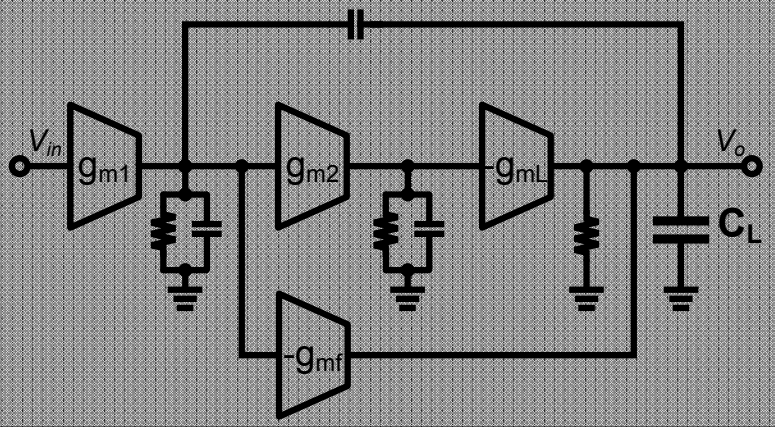


Prior Arts

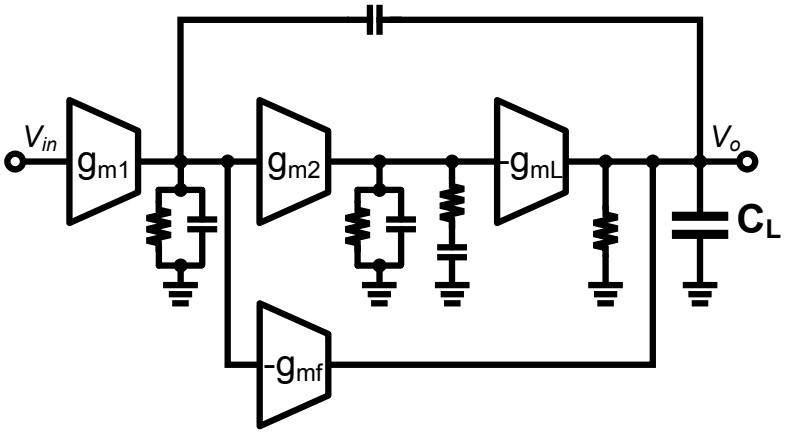
NMC [J. H. Huijsing JSSC 1985]



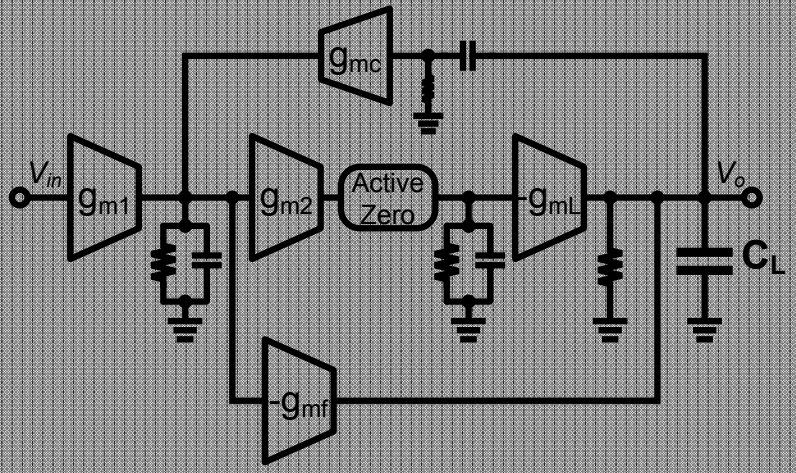
SMFFC [X. Fan JSSC 2005]



IAC [X. Peng JSSC 2011]

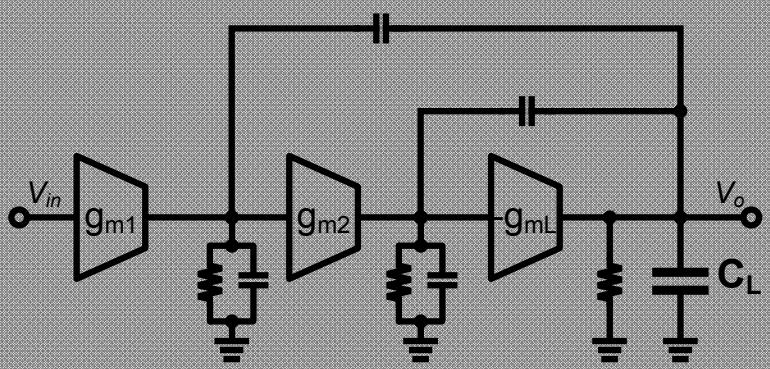


AZC [Z. Yan ISSCC 2012]

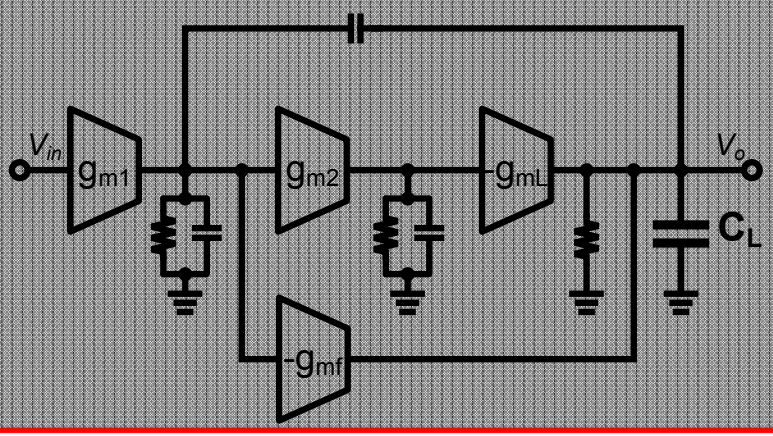


Prior Arts

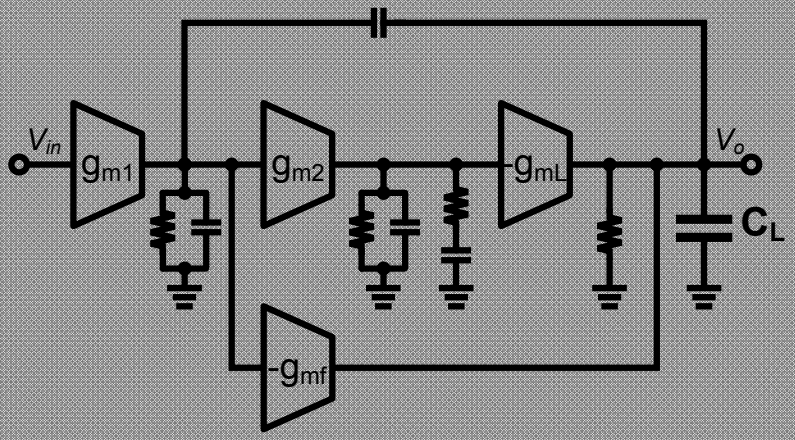
NMC [J. H. Huijsing JSSC 1985]



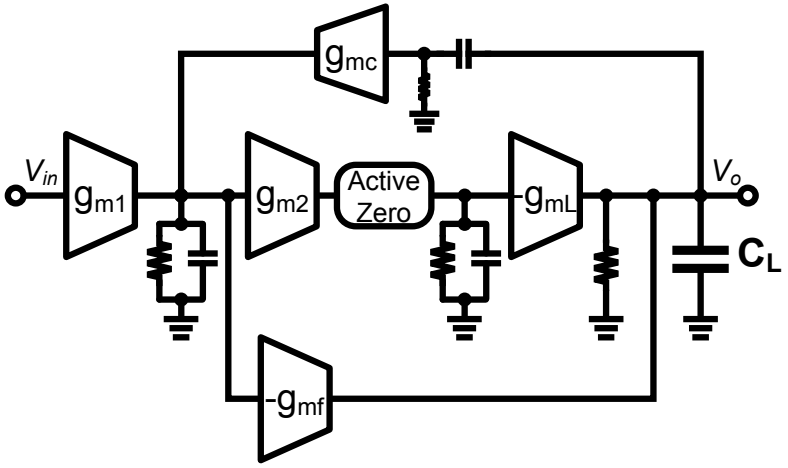
SMFFC [X. Fan JSSC 2005]



IAC [X. Peng JSSC 2011]

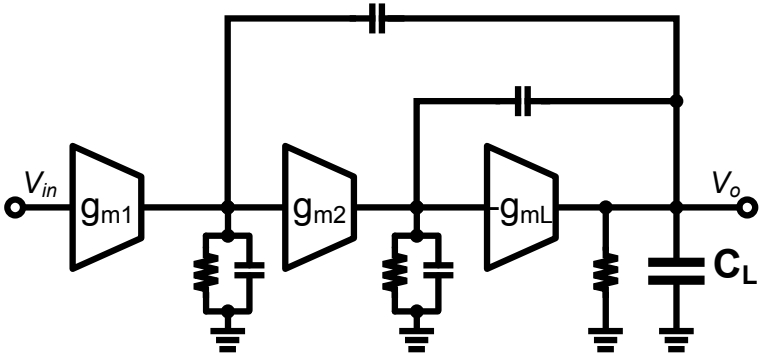


AZC [Z. Yan ISSCC 2012]

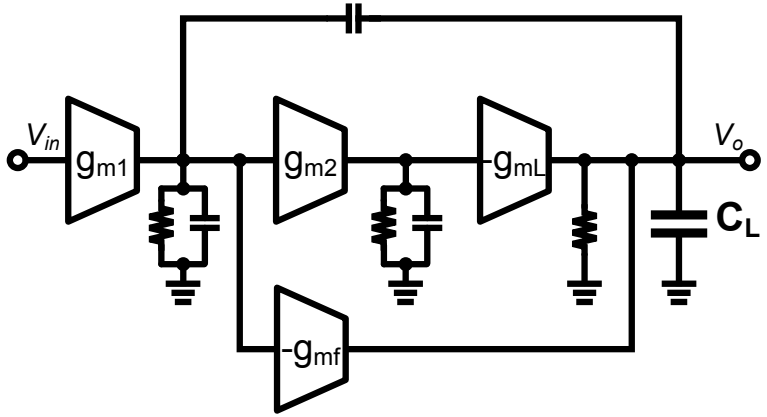


Is There An Intuitive Solution?

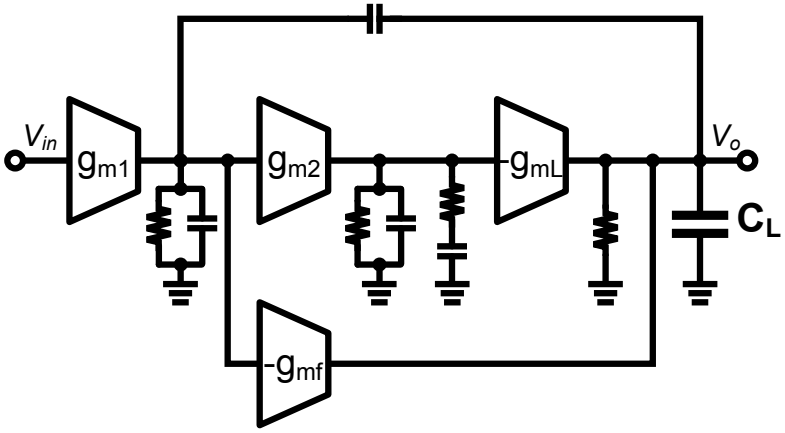
NMC [J. H. Huijsing JSSC 1985]



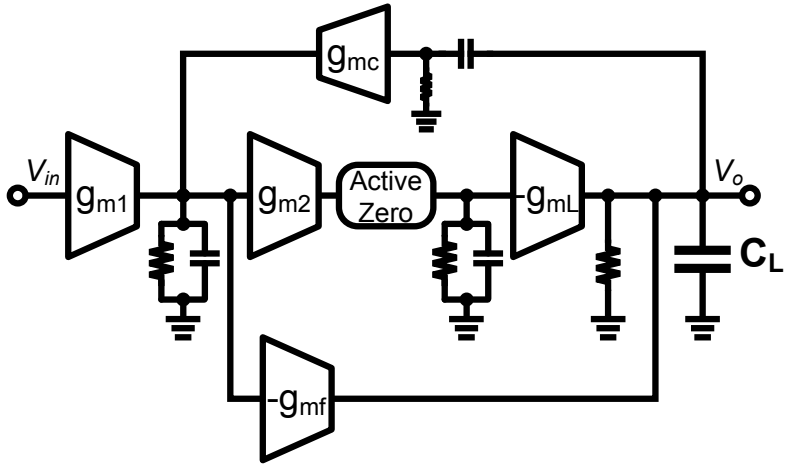
SMFFC [X. Fan JSSC 2005]



IAC [X. Peng JSSC 2011]



AZC [Z. Yan ISSCC 2012]



Features of This Paper

1. **A design-oriented-analysis method for Miller compensation.**

   Provide an intuitive solution.

   Simplifies design process.

   Improves insight for the poles.

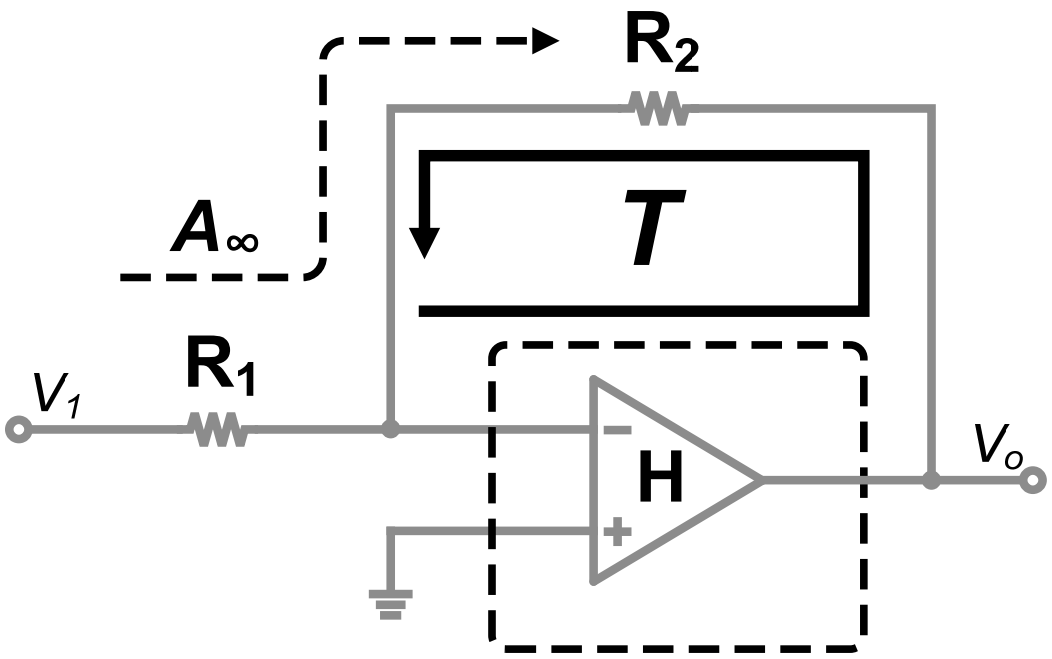
2. **A circuit implementation.**

   Achieves highest Figures-of-Merit to date.

Miller Effect: A Result of Feedback

Miller compensation can be analyzed using feedback theory.

Basic Feedback Theory



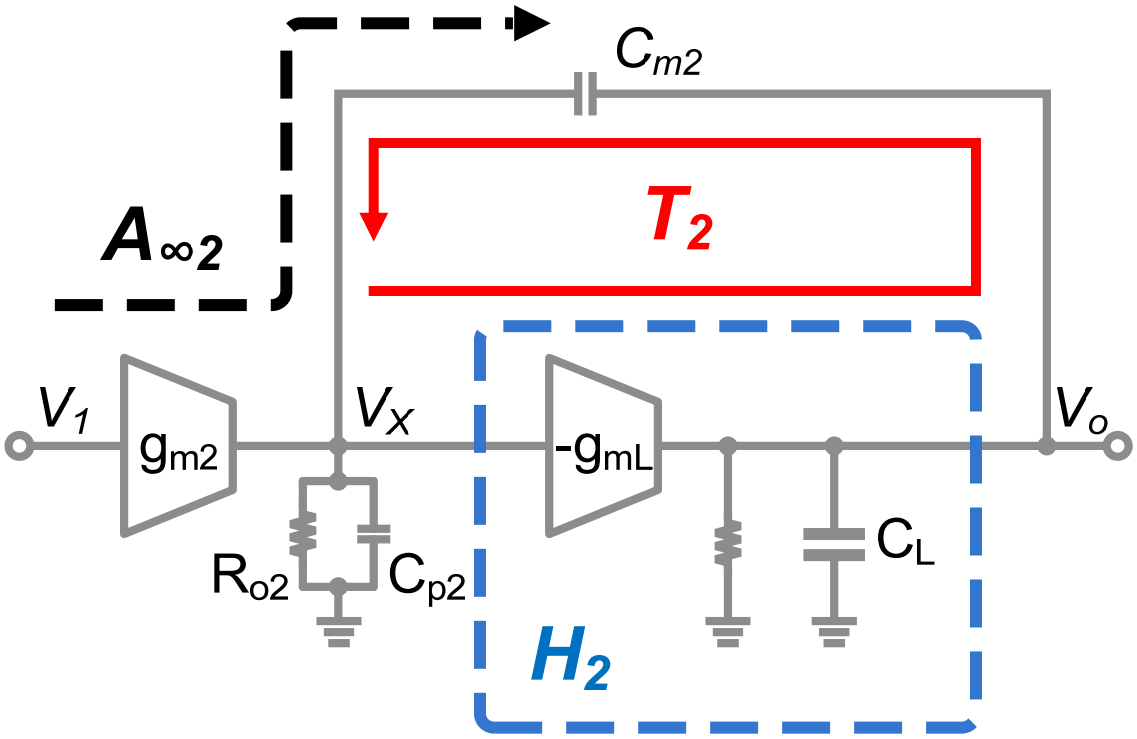
H: Plant.

T: Loop gain.

$A_\infty = -R_2/R_1$

Ideal closed-loop gain when T=∞.

$$\frac{V_O(s)}{V_1(s)} = A_\infty \frac{T}{1+T} + \frac{A_0}{1+T} \approx A_\infty \frac{T}{1+T}$$



H_2: Plant.

T_2: Loop gain.

$$A_{\infty 2} = -g_{m2}/sC_{m2}$$

$$\frac{V_O(s)}{V_1(s)} = A_{\infty 2}\frac{T_2}{1+T_2} + \frac{A_0}{1+T_2} \approx A_{\infty 2}\frac{T_2}{1+T_2}$$

when $C_L >> C_{m2}$

$$T_2 = H_2 \cdot \frac{(R_{O2} \| 1/sC_{p2})}{(R_L \| 1/sC_L) + 1/sC_m + (R_{O2} \| 1/sC_{p2})}$$

Still complicated!

Only focus on the high frequency part of T_2 (because bandwidth, gain/phase margins only depend on the behavior around GBW freq.)

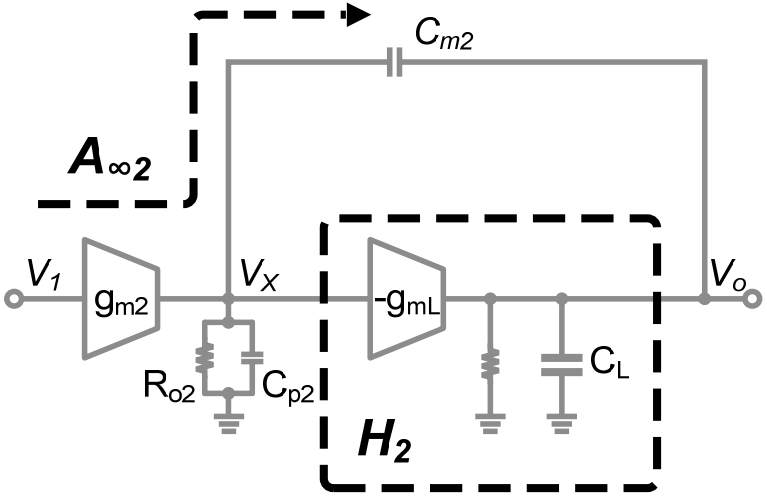
$$\lim_{f \to GBW} T_2 = T_{2\_HF} = H_2$$

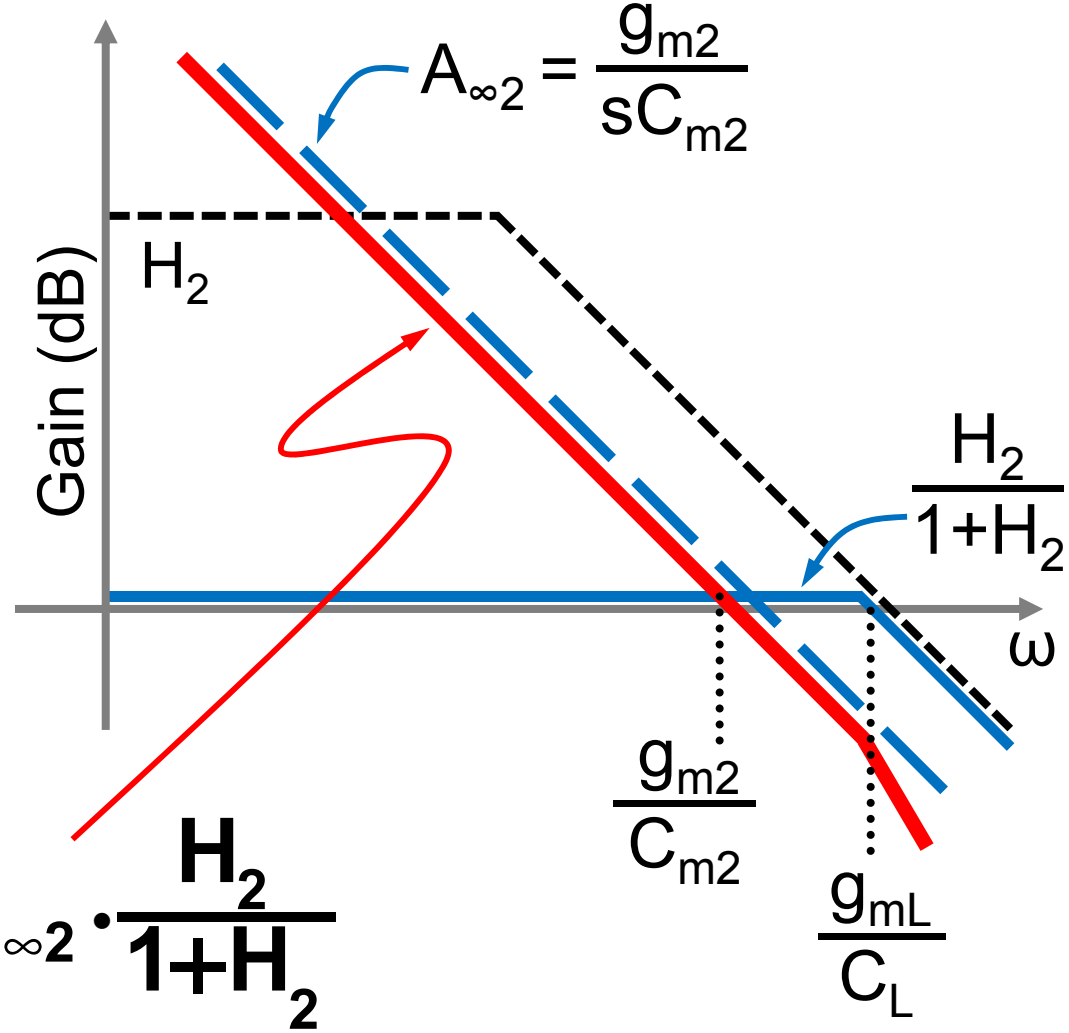
$$\left.\frac{V_O(s)}{V_1(s)}\right|_{HF} = A_{\infty 2}\frac{T_2}{1+T_2} \approx A_{\infty 2}\cdot\frac{H_2}{1+H_2}$$

Ideal single pole.

Band-limiting pole (Unity-feedback of H_2).

2-Stage:

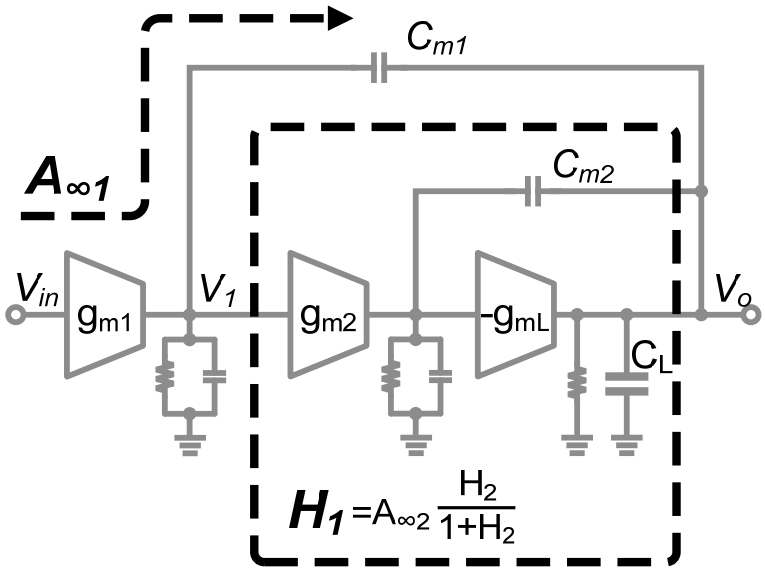


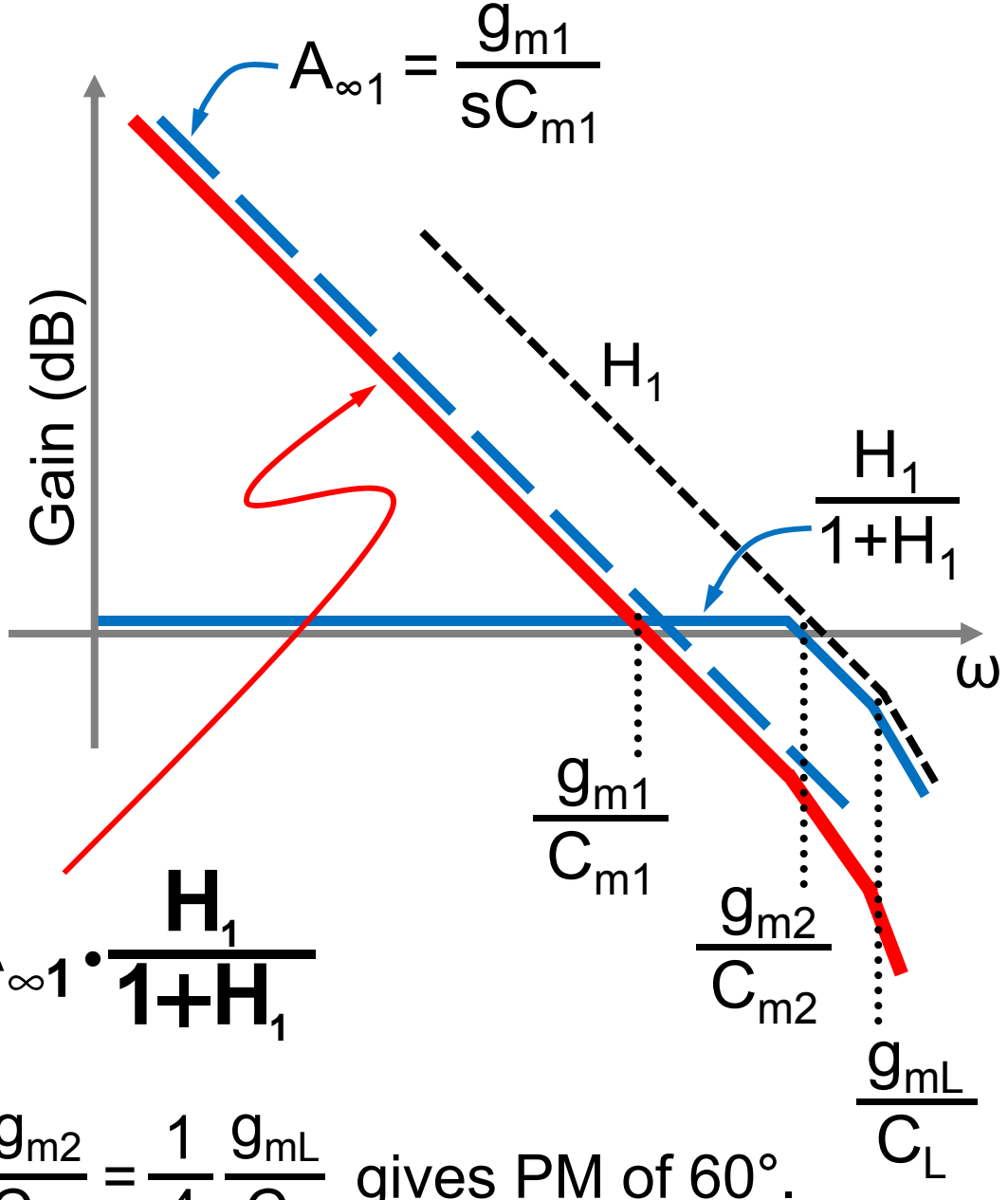


$$\left.\frac{V_o}{V_1}\right|_{HF} = A_{\infty 2} \cdot \frac{H_2}{1+H_2}$$

Setting GBW = $\frac{g_{m2}}{C_{m2}} = \frac{1}{2}\frac{g_{mL}}{C_L}$ gives PM of 60°.

3-Stage:

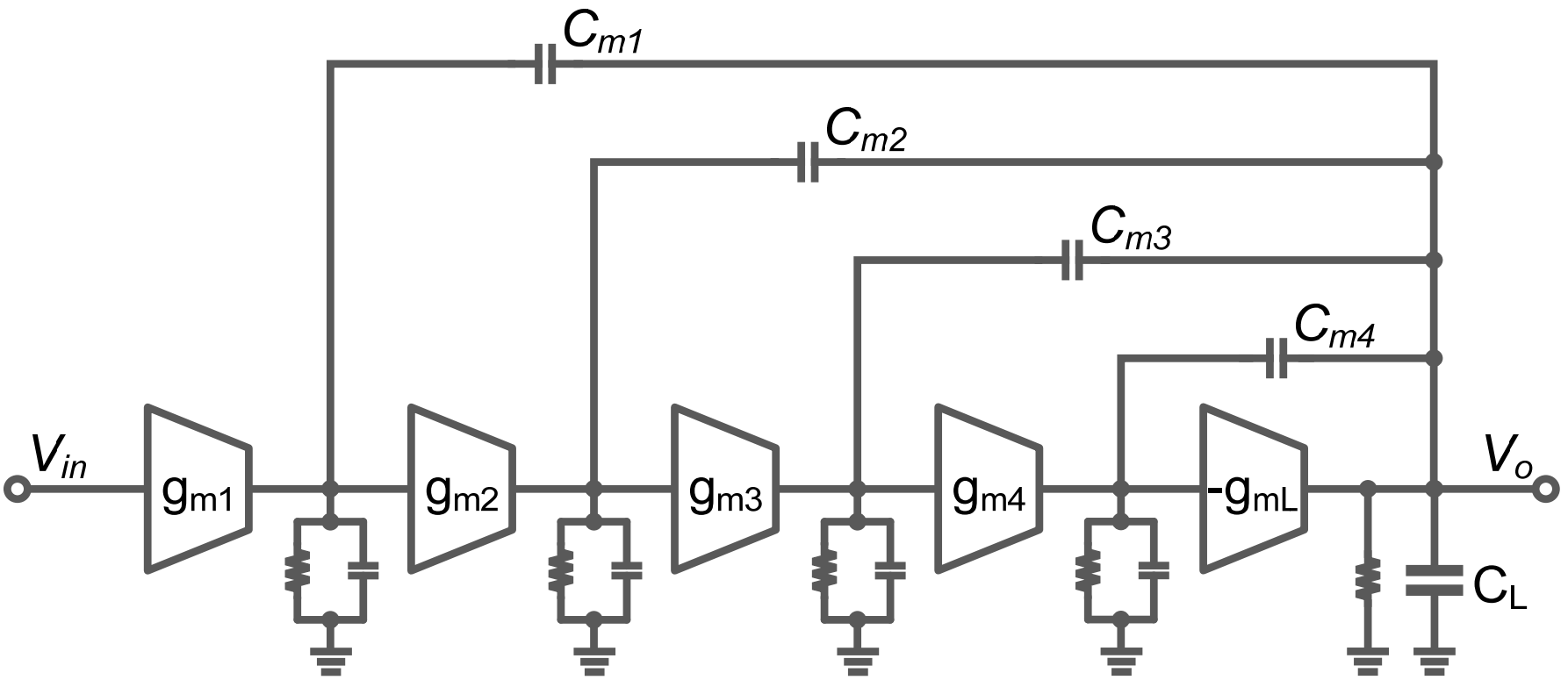




$$\left.\frac{V_o}{V_{in}}\right|_{HF} = A_{\infty 1} \cdot \frac{H_1}{1+H_1}$$

Setting GBW $= \frac{g_{m1}}{C_{m1}} = \frac{1}{2}\frac{g_{m2}}{C_{m2}} = \frac{1}{4}\frac{g_{mL}}{C_L}$ gives PM of 60°.

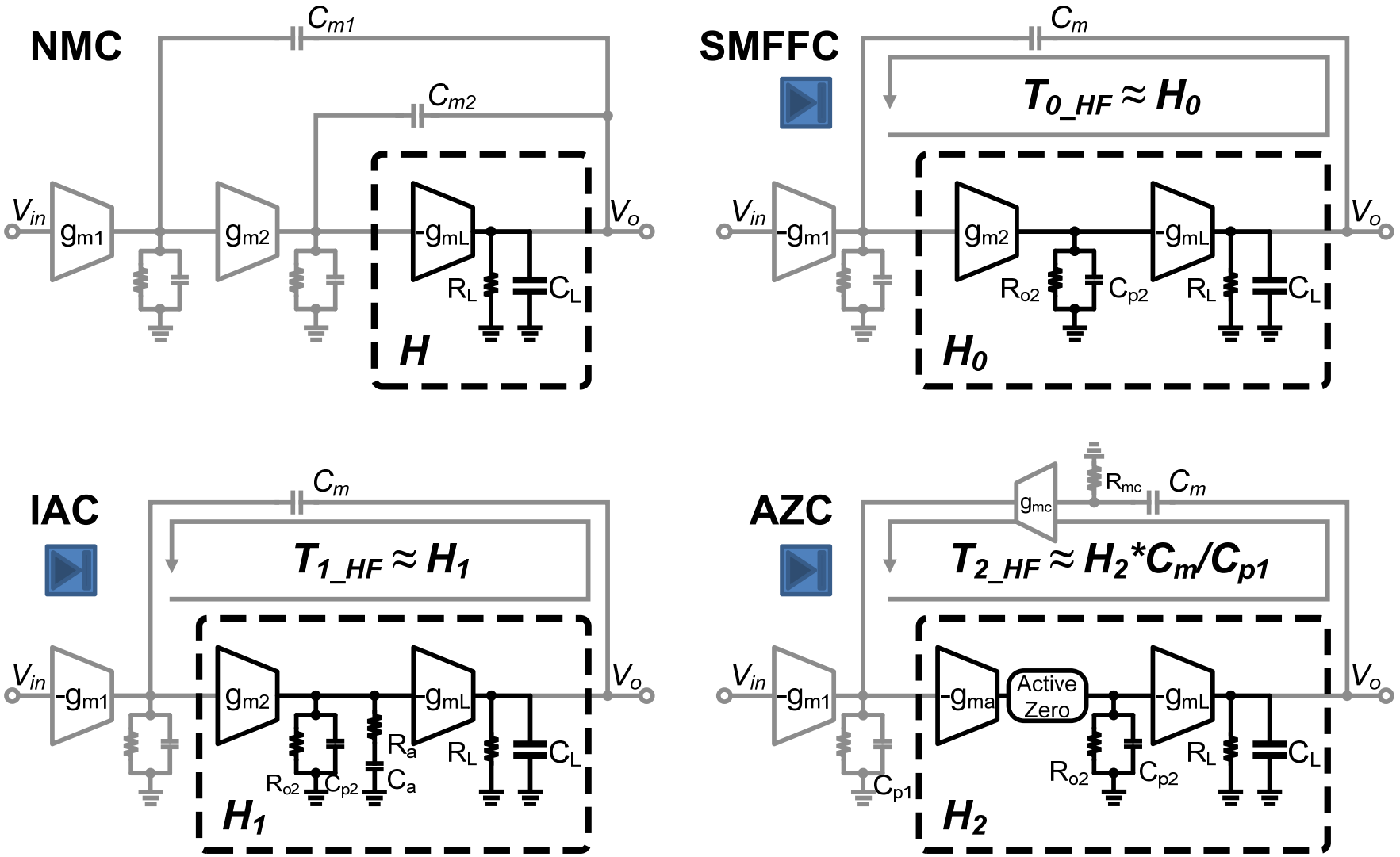
Apply the Method Recursively

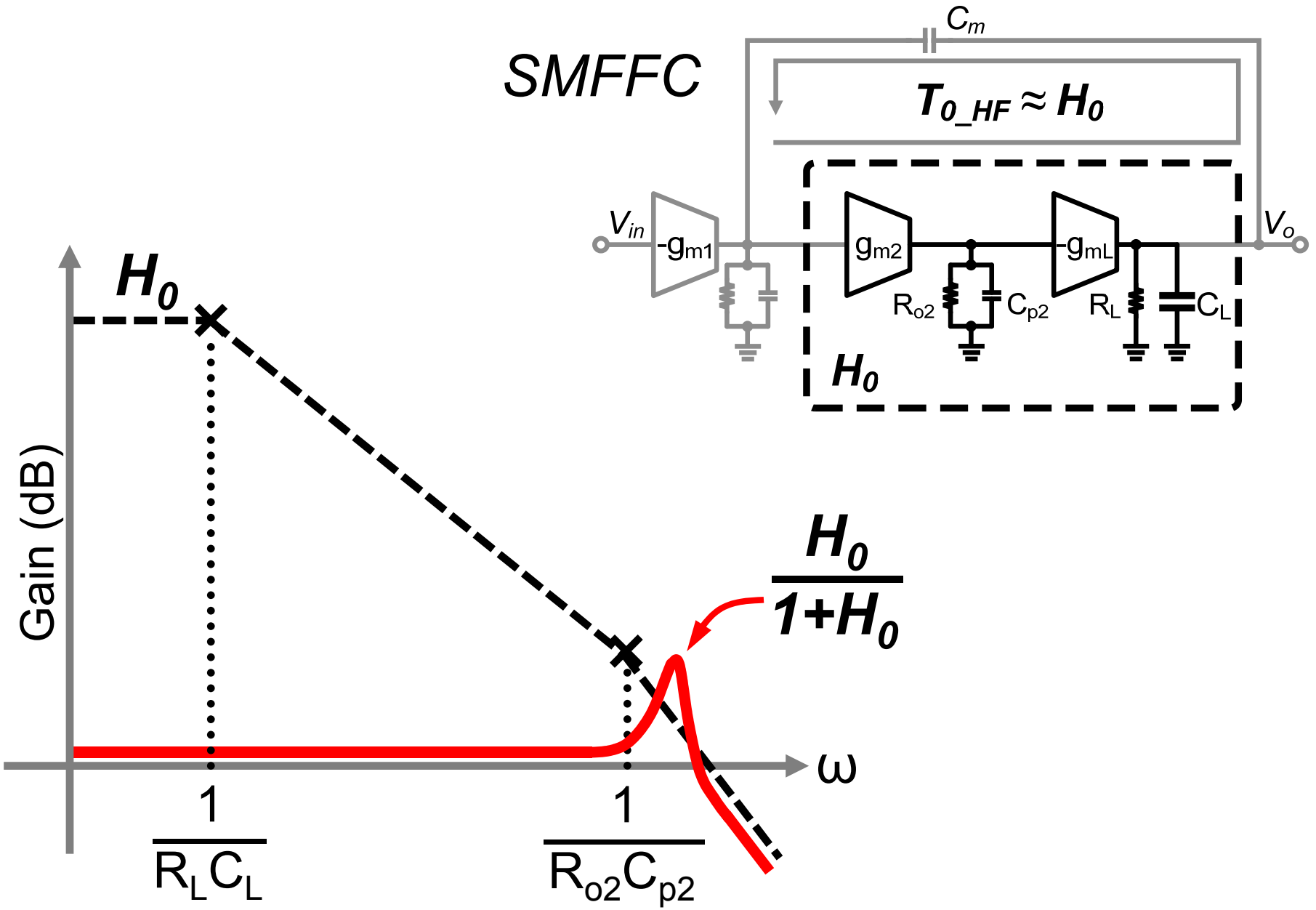


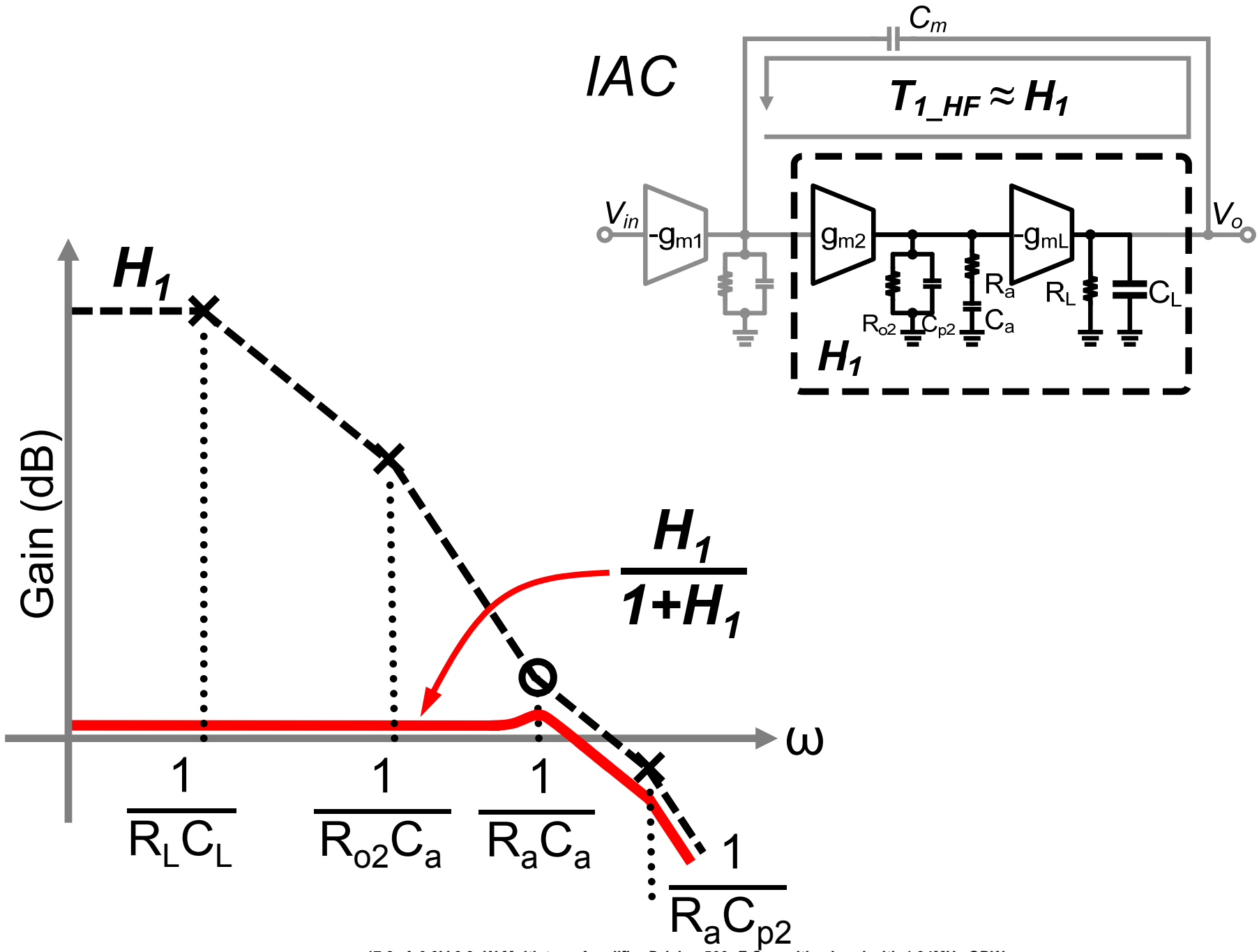
$$\text{GBW} = \frac{g_{m1}}{C_{m1}} = \frac{1}{2}\frac{g_{m2}}{C_{m2}} = \frac{1}{3.2}\frac{g_{m3}}{C_{m3}} = \frac{1}{5.2}\frac{g_{m4}}{C_{m4}} = \frac{1}{10.4}\frac{g_{mL}}{C_L}$$

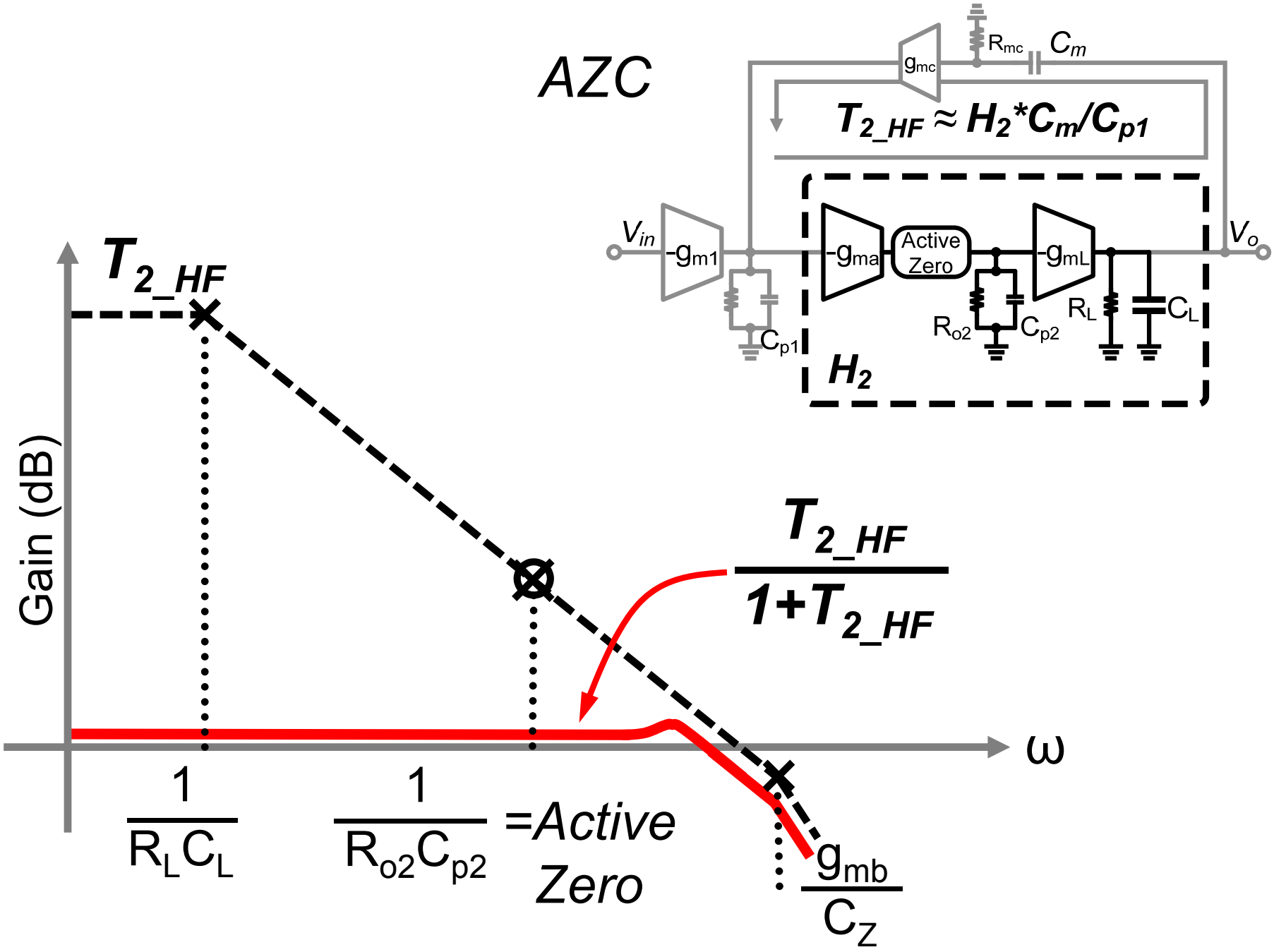
5th-order Butterworth frequency response.

Prior Arts:
3-Stage Design → 2-Stage Design



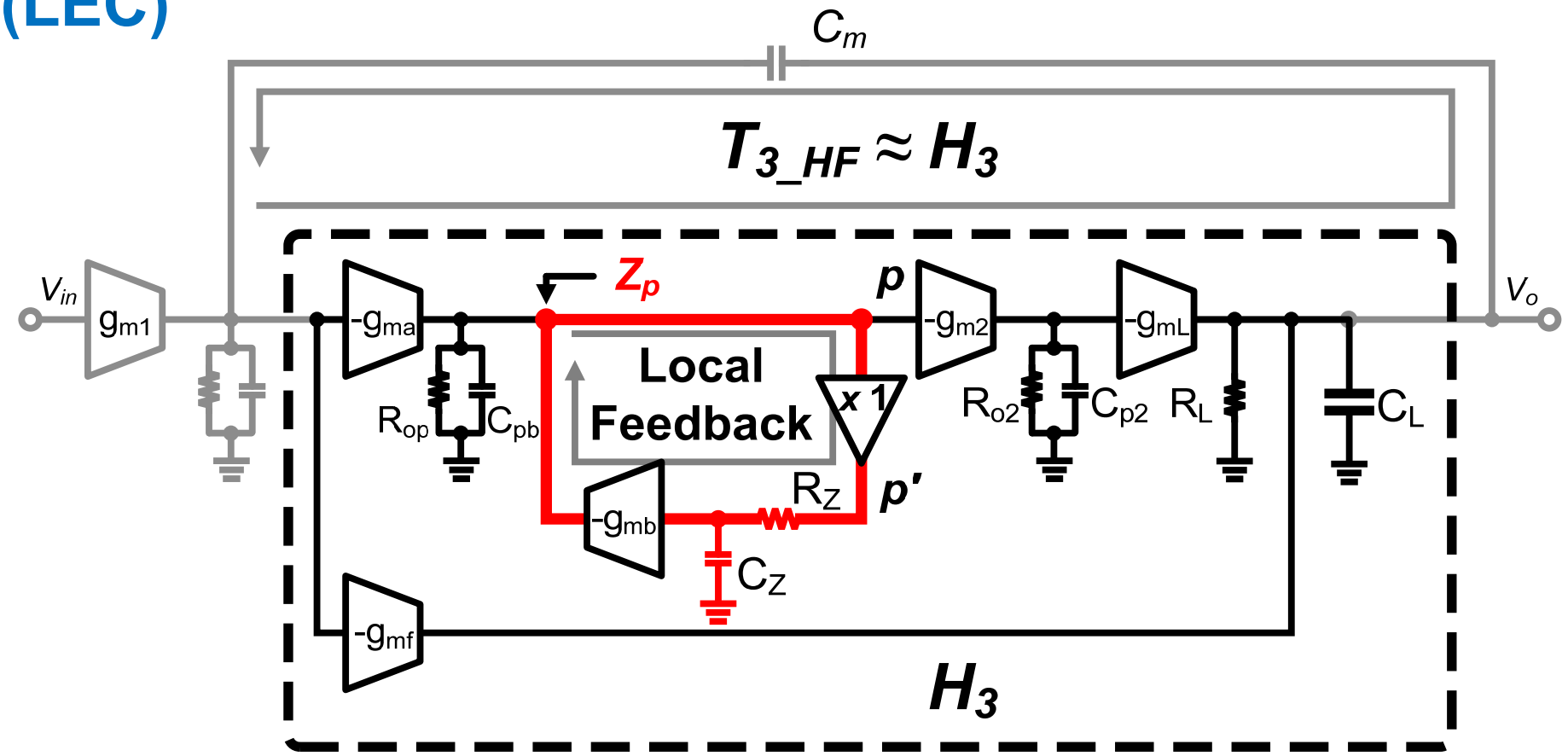




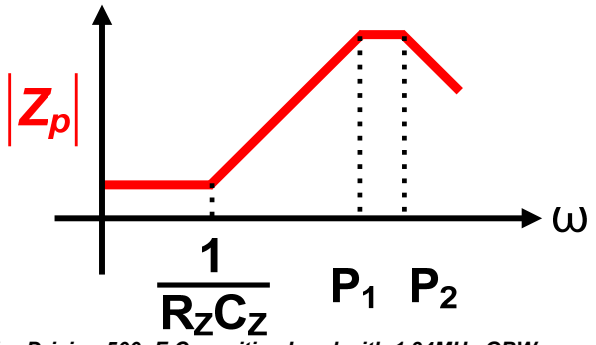


Proposed Local-Feedback-Enhanced Compensation (LEC)

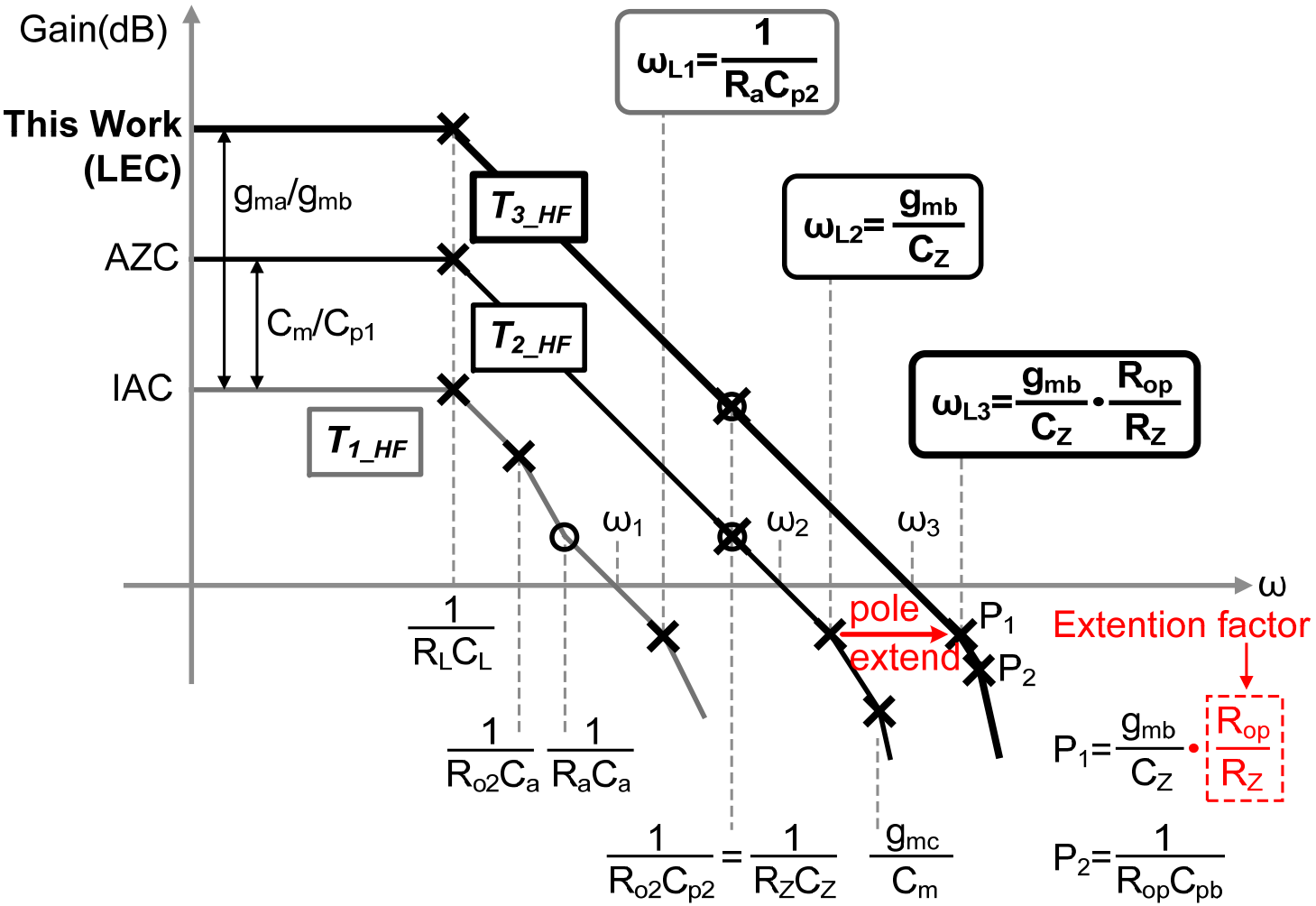
Proposed Local-Feedback-Enhanced Compensation (LEC)



$$Z_p \approx \frac{1+sR_ZC_Z}{g_{mb}+sC_ZR_Z/R_{op}+s^2R_ZC_ZC_{pb}}$$

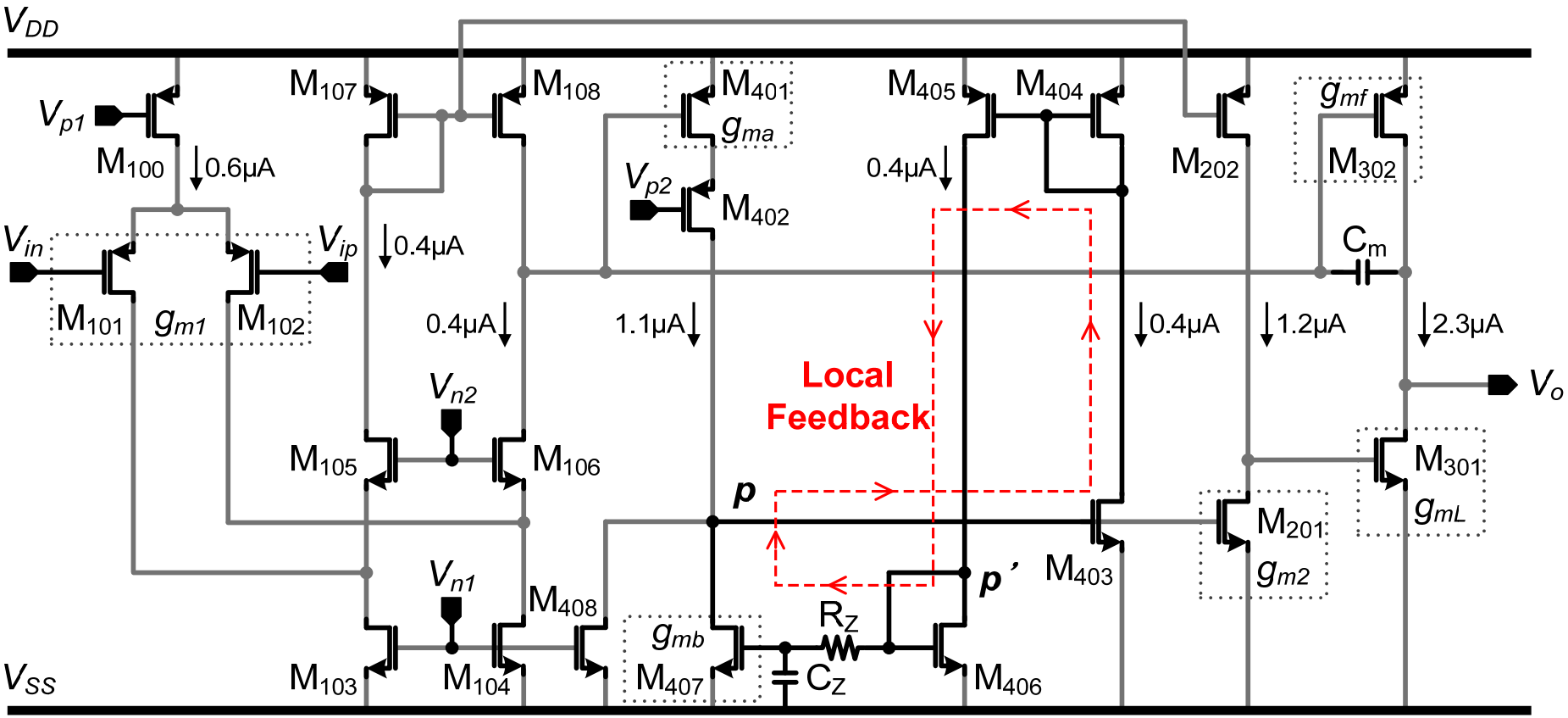


Simplified Bode Plot of Miller Loop



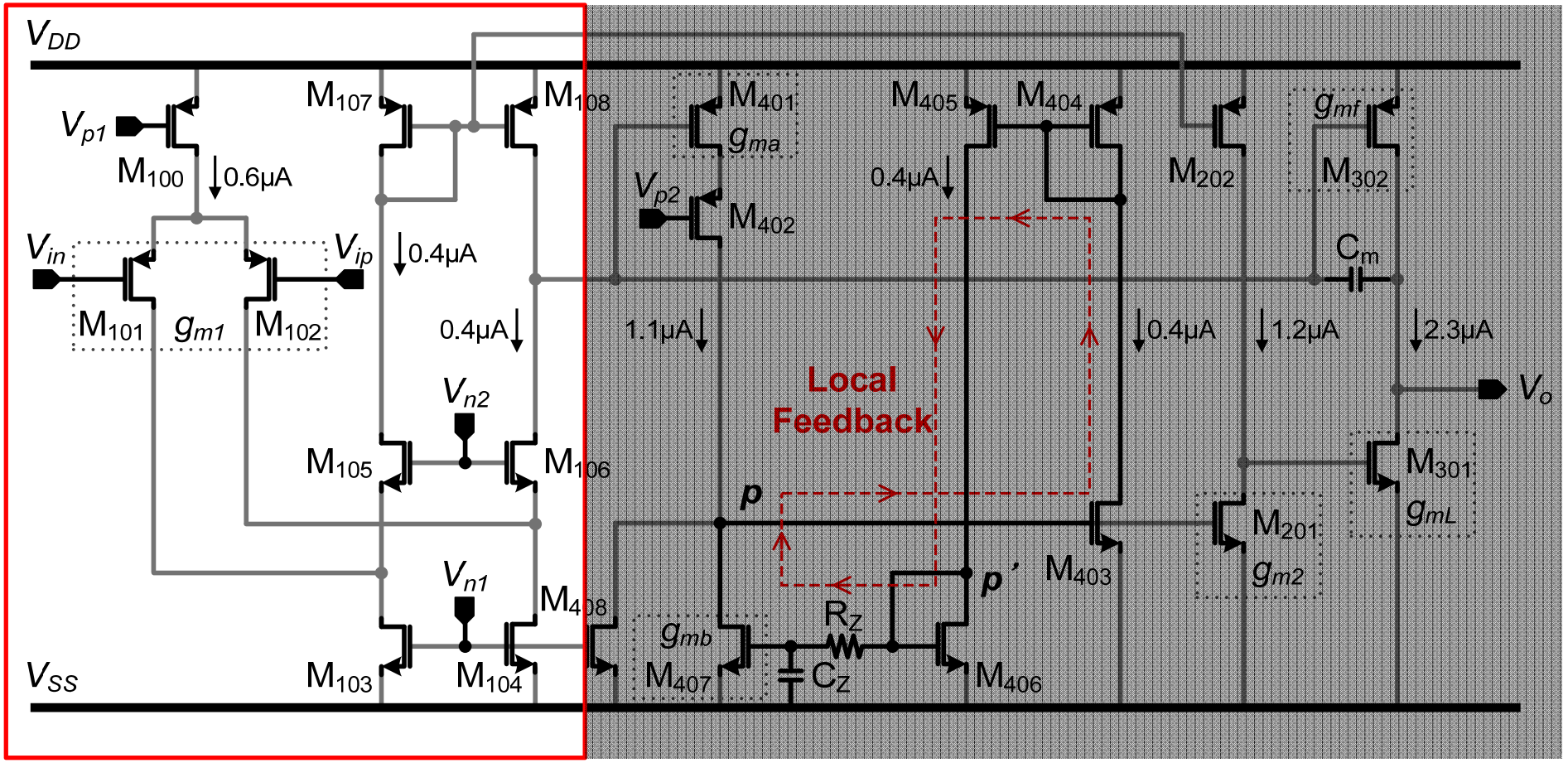
$$\omega_1 = g_{m2}R_a\frac{g_{mL}}{C_L} \qquad \omega_2 = \frac{g_{ma}R_ZC_mC_Z}{C_{p1}C_{p2}}\frac{g_{mL}}{C_L} \qquad \omega_3 = \frac{g_{ma}g_{m2}R_ZC_Z}{g_{mb}C_{p2}}\frac{g_{mL}}{C_L}$$

Circuit Implementation

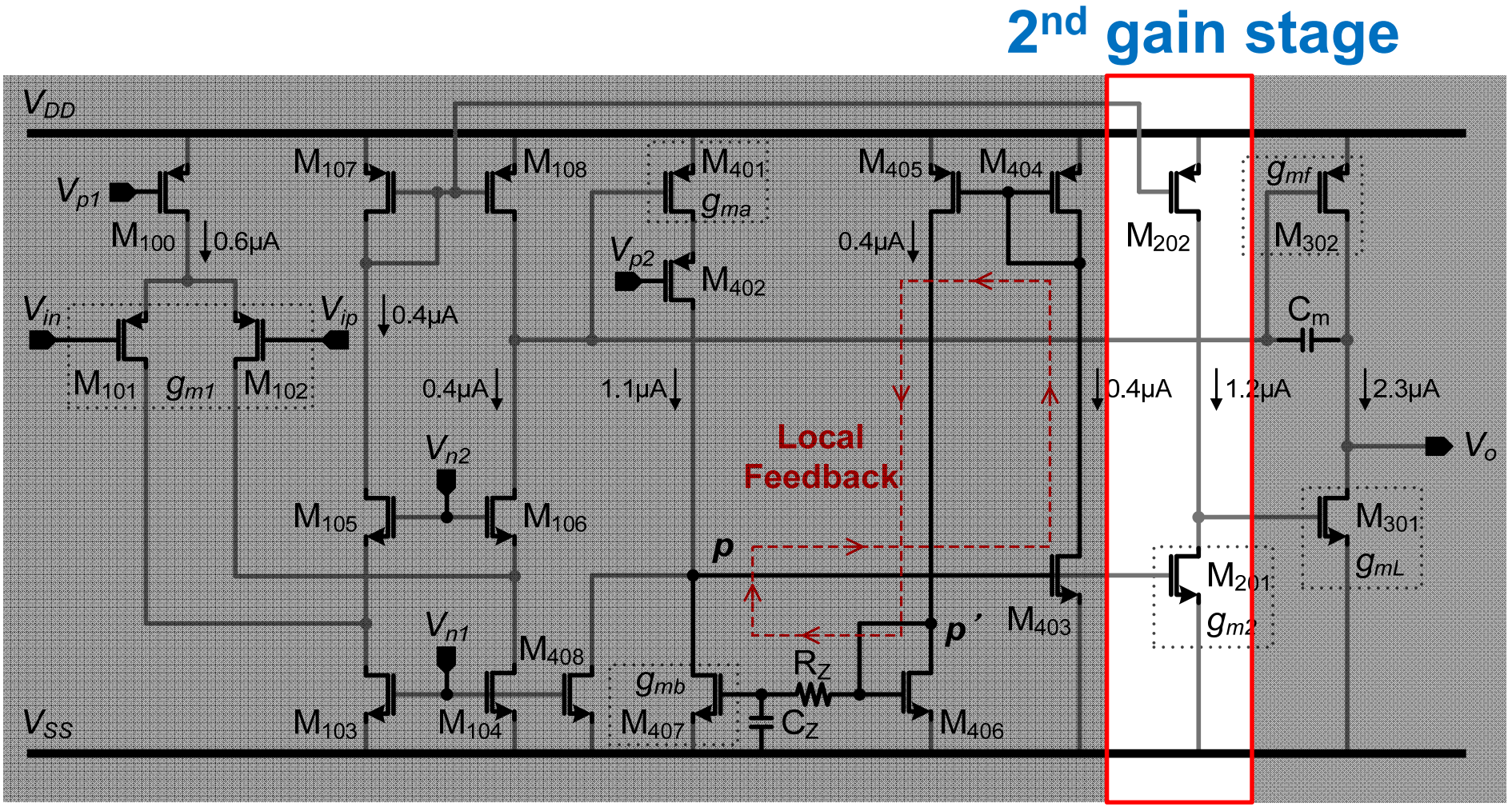


Circuit Implementation

1st gain Stage

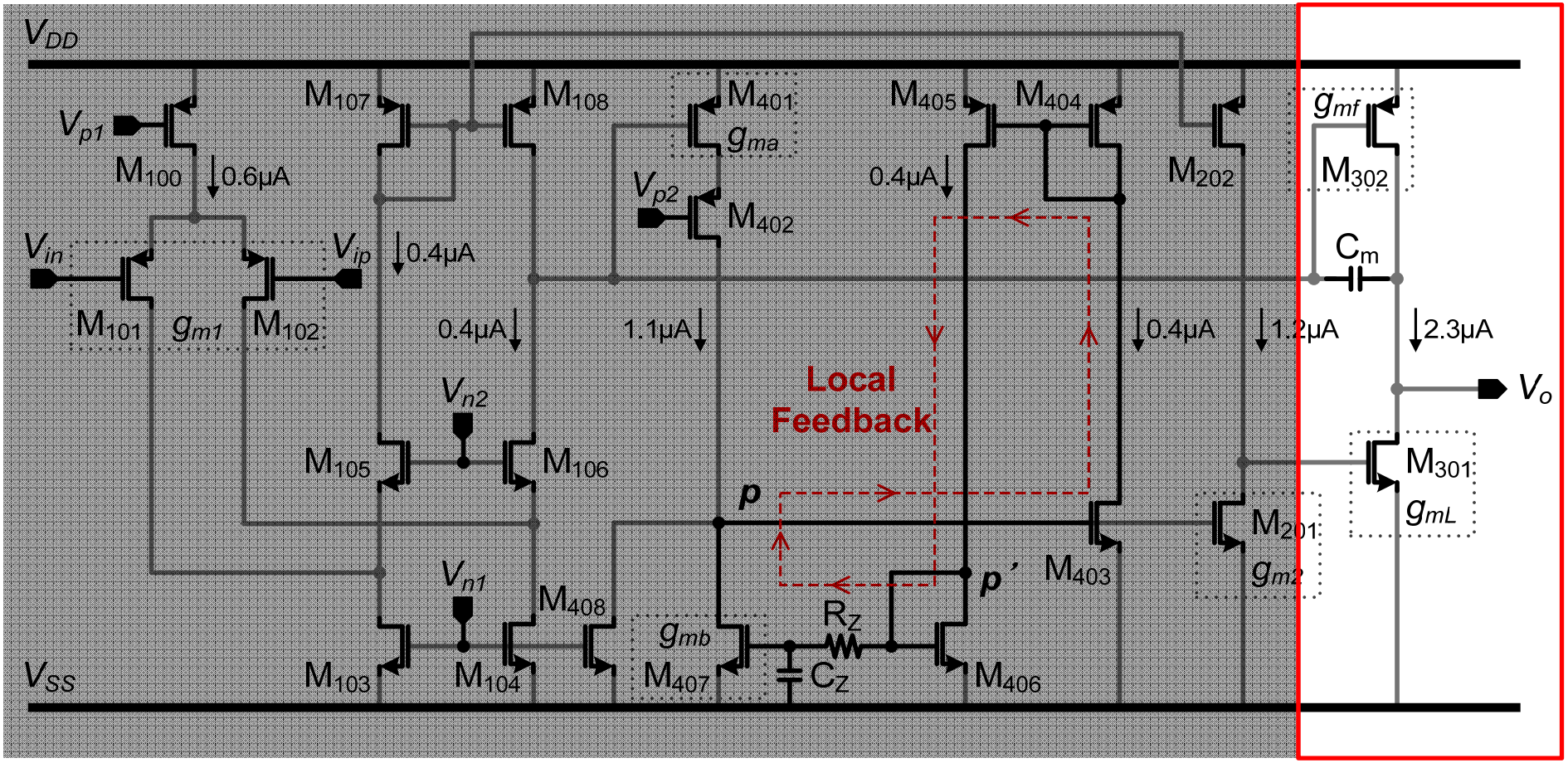


Circuit Implementation



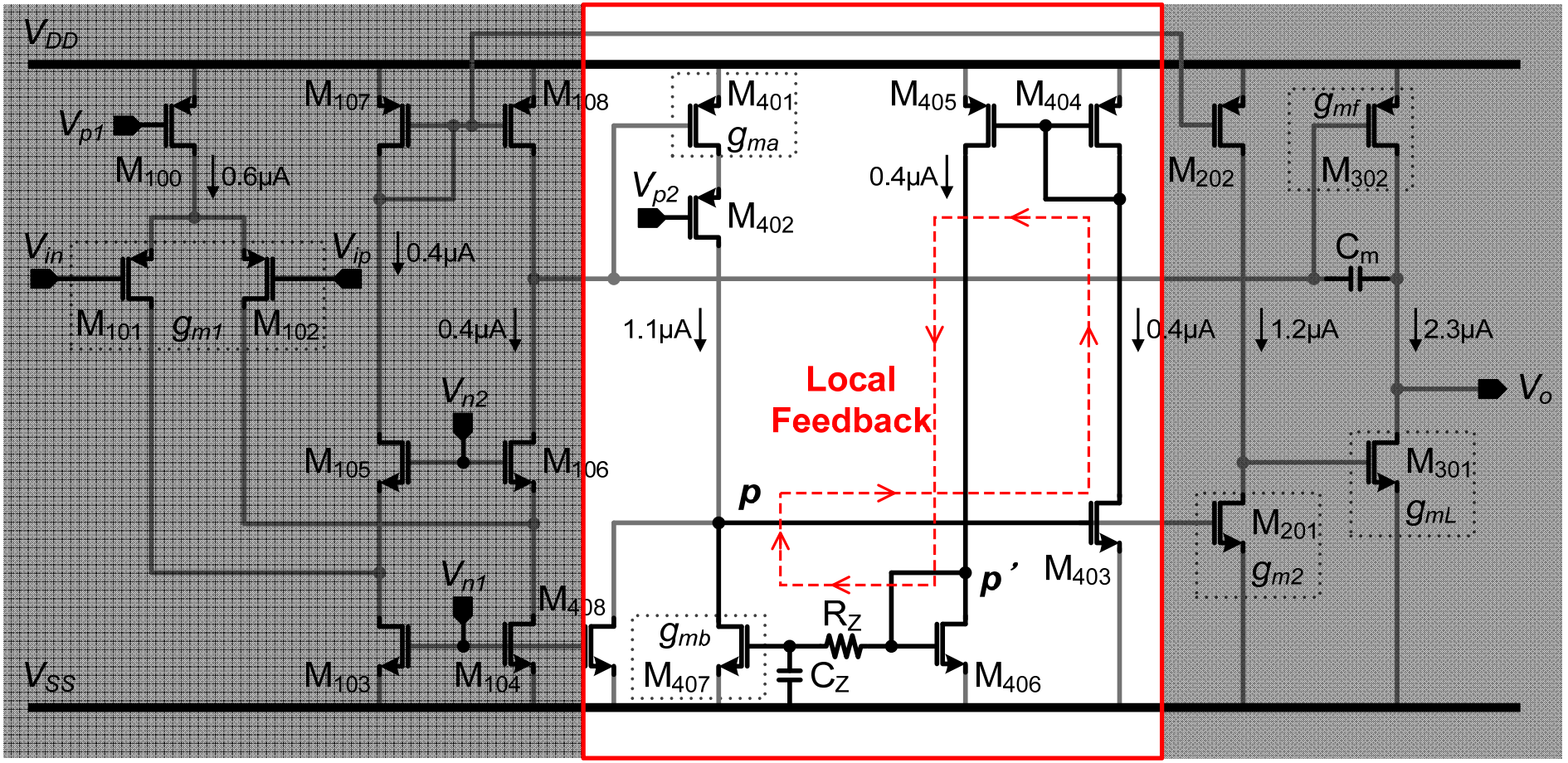
Circuit Implementation

3rd gain stage

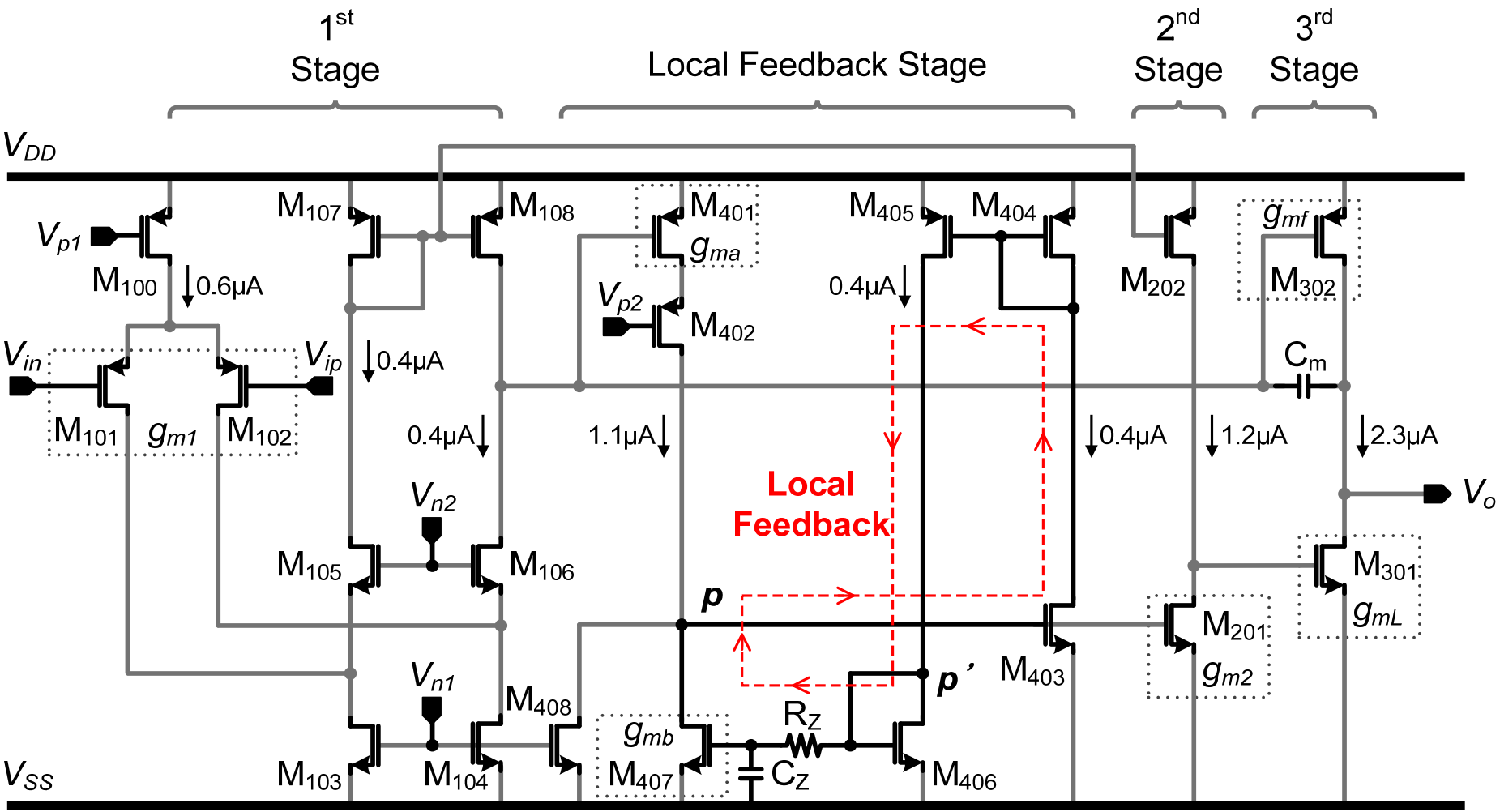


Circuit Implementation

Local Feedback Stage

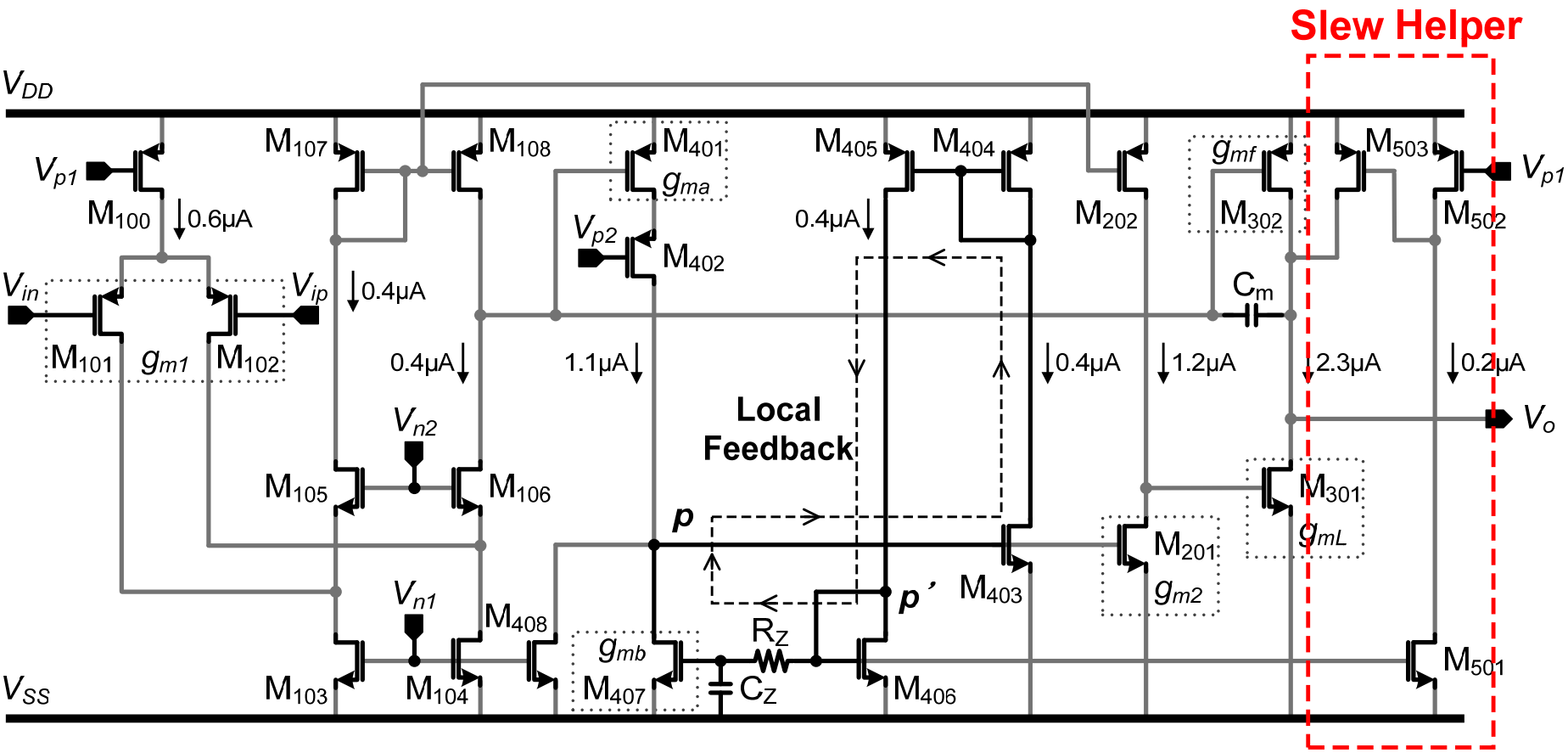


Circuit Implementation



Almost done, but transient needs to be improved.

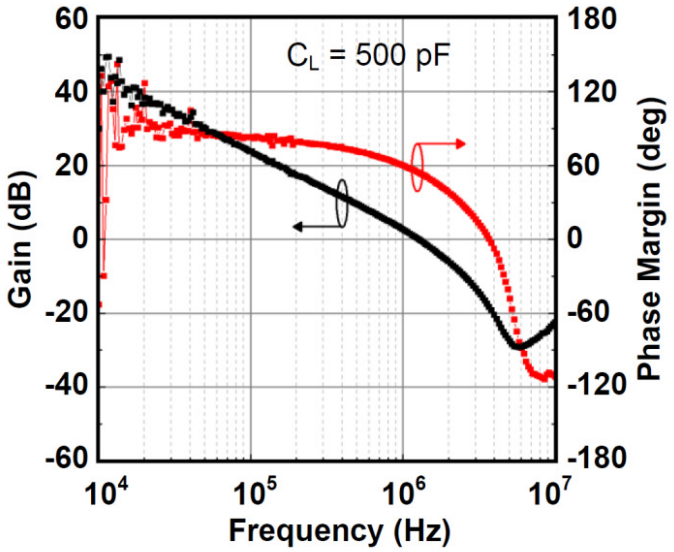
Circuit Implementation – Final

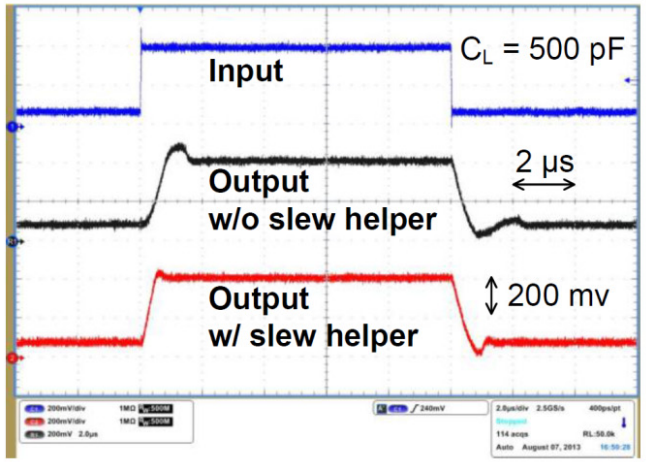


Minimum supply = $1V_{GS} + 2\ V_{DSAT}$

Can be easily reduced to $1V_{GS} + 1\ V_{DSAT}$

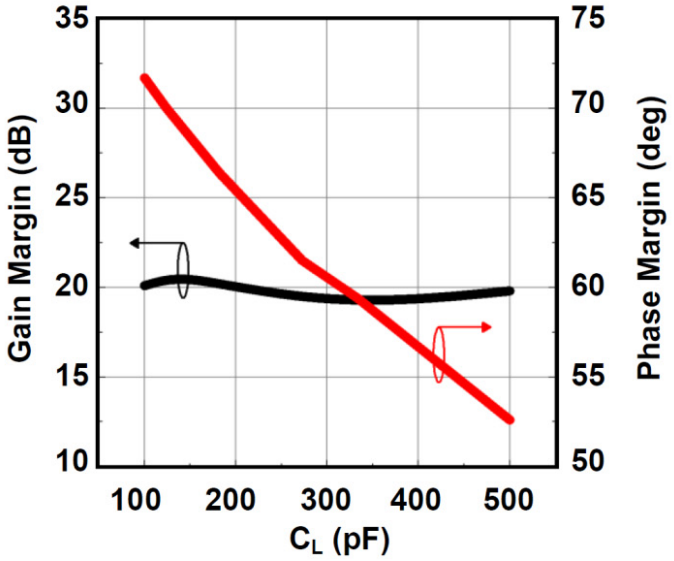
Measurement Results

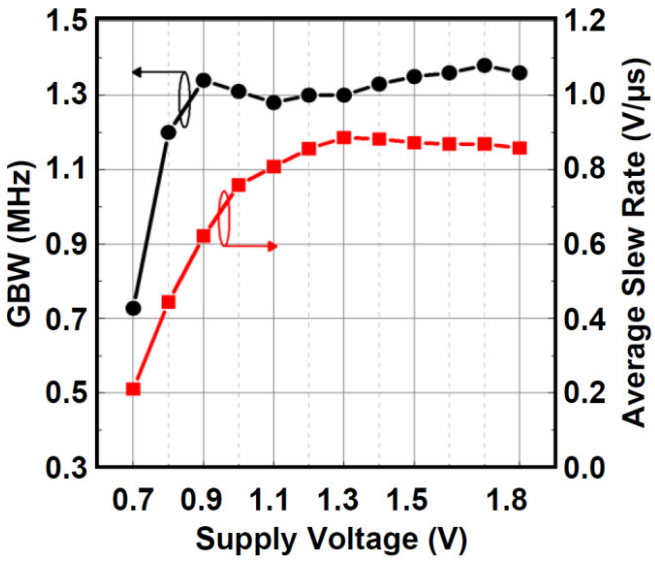




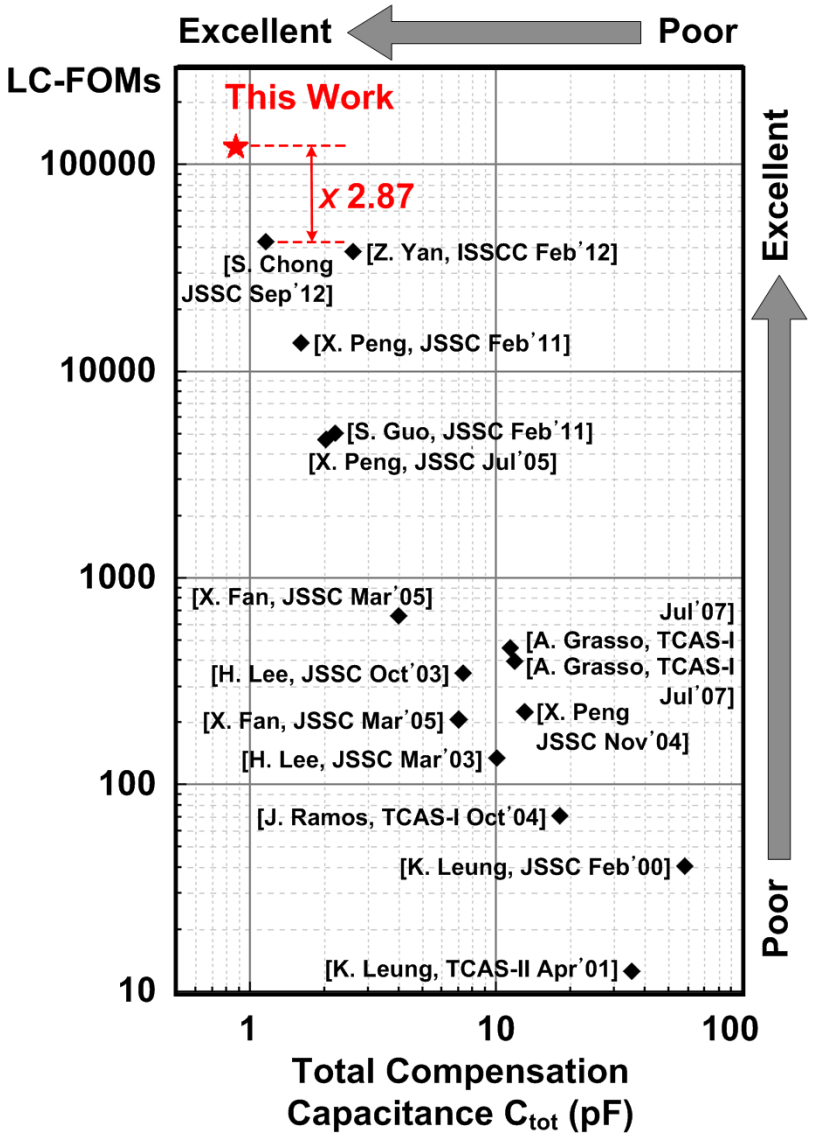
w/o: +SR=0.44V/µs -SR=0.53V/µs +T_s=2.57µs -T_s=2.48µs (1%)

w/: +SR=0.71V/µs -SR=0.53V/µs +T_s=0.82µs -T_s=1.42µs (1%)





Comparison Table



	[1] X. Peng JSSC Feb'11	[2] Z. Yan ISSCC Feb'12	This Work
Supply Voltage V_{DD} (V)	1.5	2	0.9
DC gain (dB)	110	>100	>100
Load C_L (pF)	150	15,000	500
GBW (MHz)	4.4	0.95	1.34
Phase Margin (deg)	57	52.3	52.7
Average SR (V/μs)	1.8	0.22	0.62
Power (μW@V_{DD})	30 @ 1.5V	144 @ 2V	6.3 @ 0.9V
Total Capacitance (pF)	1.6	2.6	0.87
Chip Area (mm^2)	0.02	0.016	0.007
Technology	0.35μm CMOS	0.35μm CMOS	0.18μm CMOS
FOM_S [(MHz·pF)/mW]	22,000	98,958	106,349
FOM_L [(V/μs·pF)/mW]	9,000	22,917	49,206
LC-FOM_S (MHz/mW)	13,750	38,061	122,240
LC-FOM_L [(V/μs)/mW]	5,625	8,814	56,559

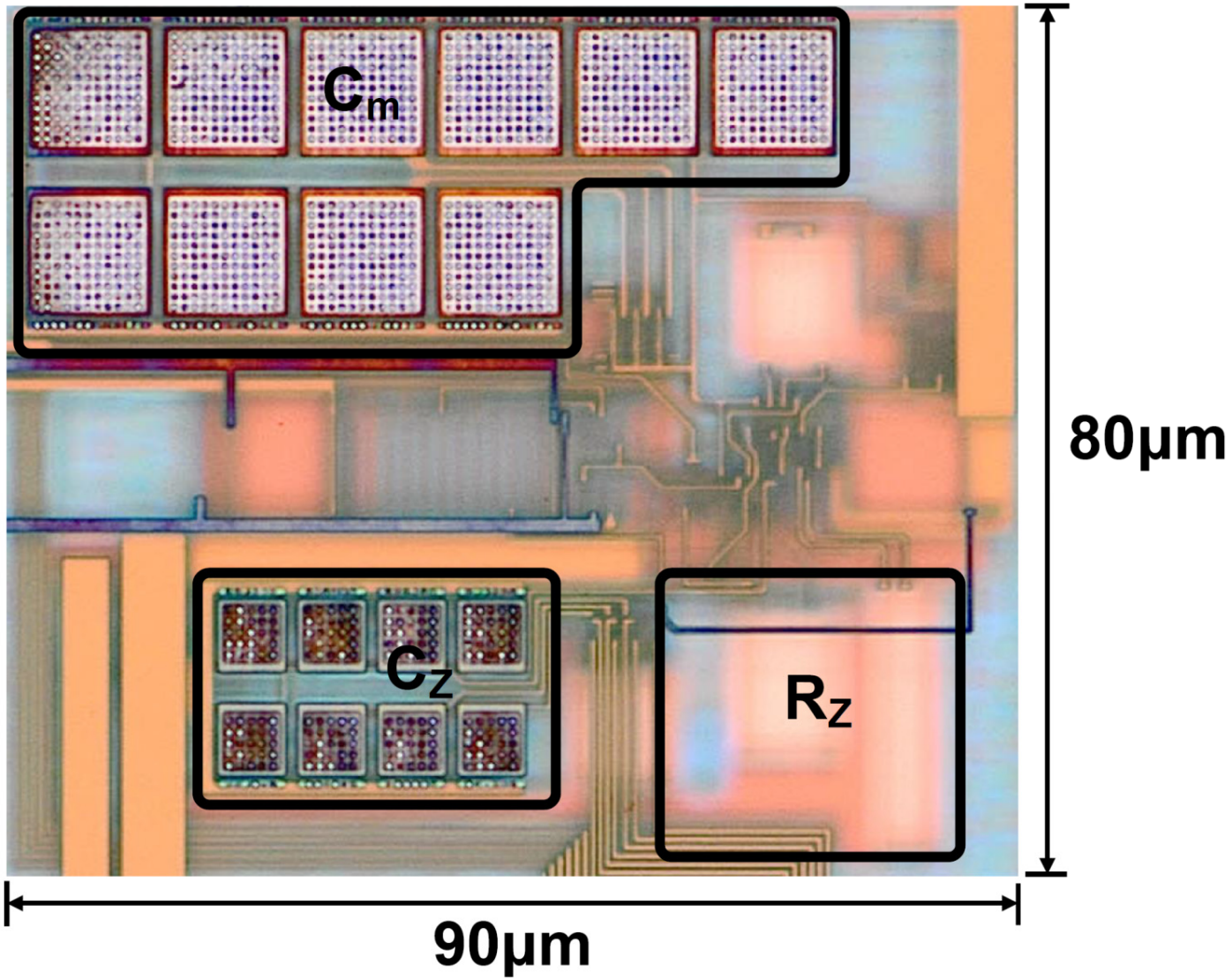
Typical FOM_S and FOM_L [1]-[2]:

$$FOM_S = \frac{GBW \cdot C_L}{Power} \qquad FOM_L = \frac{SR \cdot C_L}{Power}$$

Large-Capacitive-Load FOM_S and FOM_L [2]:

$$\text{LC-}FOM_S = \frac{GBW}{Power} \cdot \frac{C_L}{C_{tot}} \qquad \text{LC-}FOM_L = \frac{SR}{Power} \cdot \frac{C_L}{C_{tot}}$$

Die Photo



Thank you!

POLITECNICO DI MILANO

DIPARTIMENTO DI ELETTRONICA, INFORMAZIONE E BIOINGEGNERIA

17.4: CMOS impedance analyzer for nanosamples investigation operating up to 150MHz with sub-aF resolution

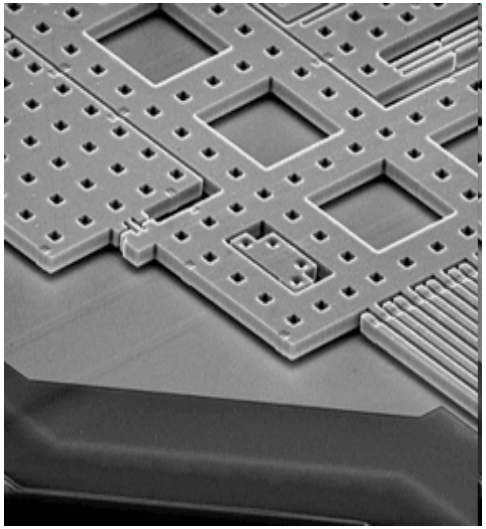
G. Ferrari, D. Bianchi, A. Rottigni, M. Sampietro

Outline

- Work motivation
- IC concept
- Implementation details
- Experimental results
- Conclusions

Impedance Sensing

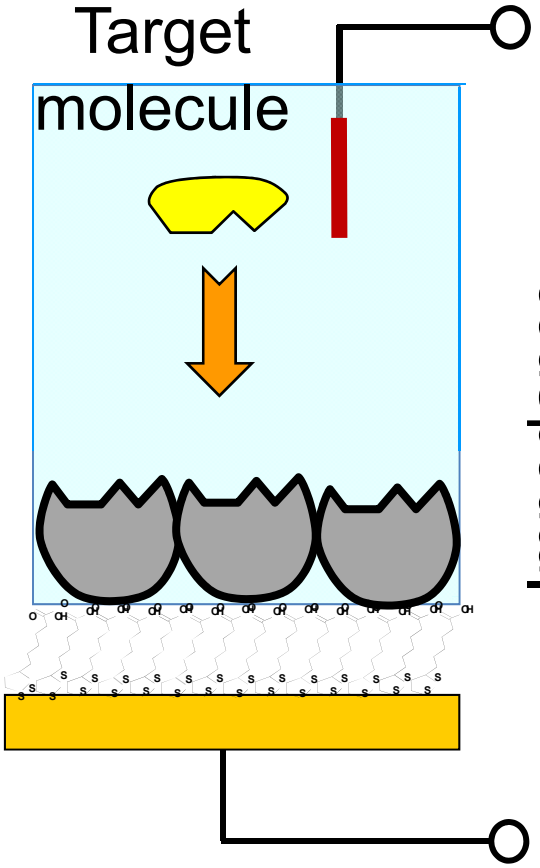
Capacitance Measurement



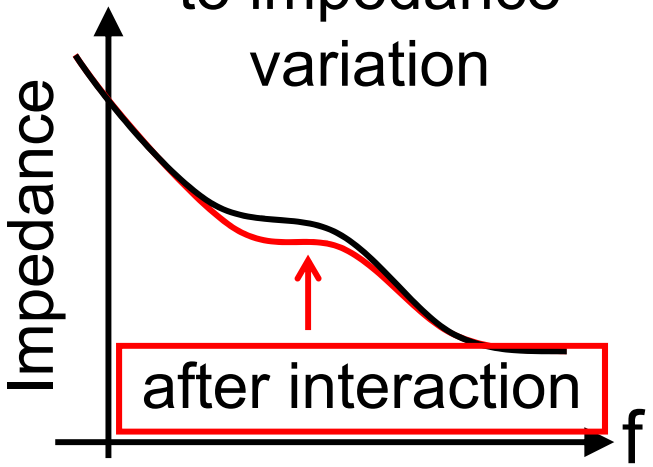
Inertial MEMS

J.A. Geen et al., *J. Solid State Cir.* **37** (2002) 1860-1866

Affinity Biosensors



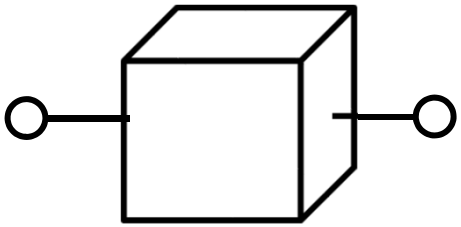
Conformational change to impedance variation



Impedance Spectroscopy

Impedance sensing at nanoscale

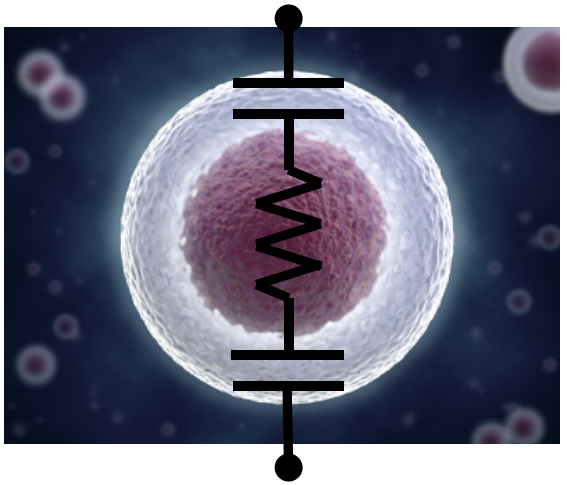
Electrical signals scale down with the electrode size!



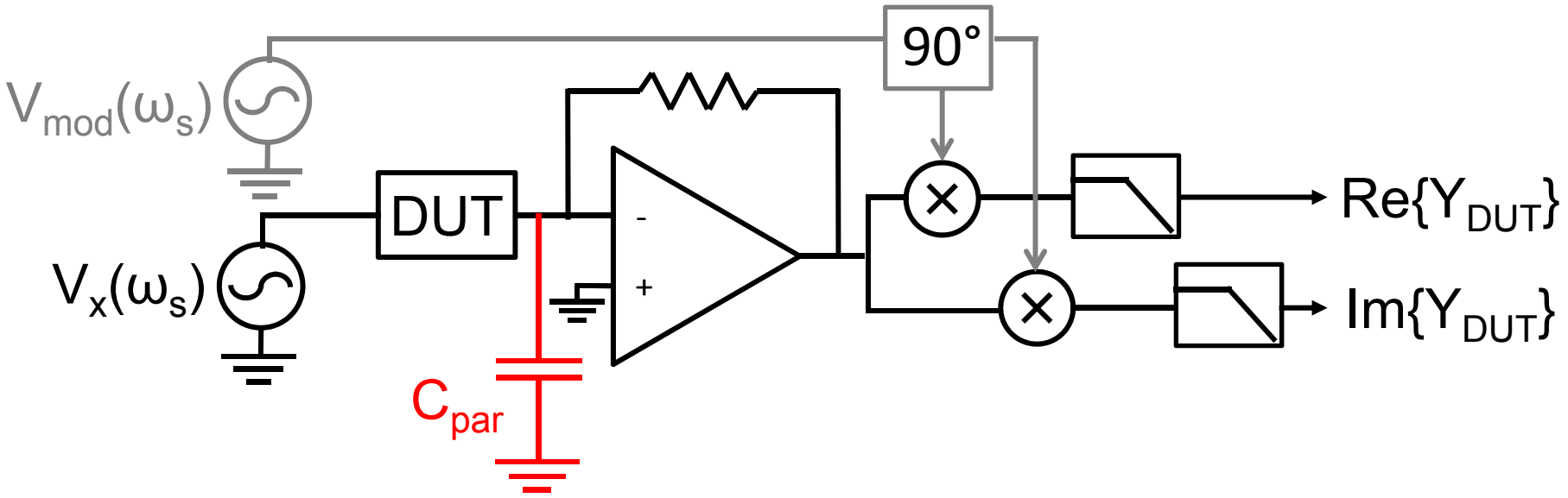
cube of semi-insulating sample
100 nm x 100 nm x 100nm

$C_{sensor} \approx$ **5aF**

- High sensitivity electronics
- Wide bandwidth spectroscopy

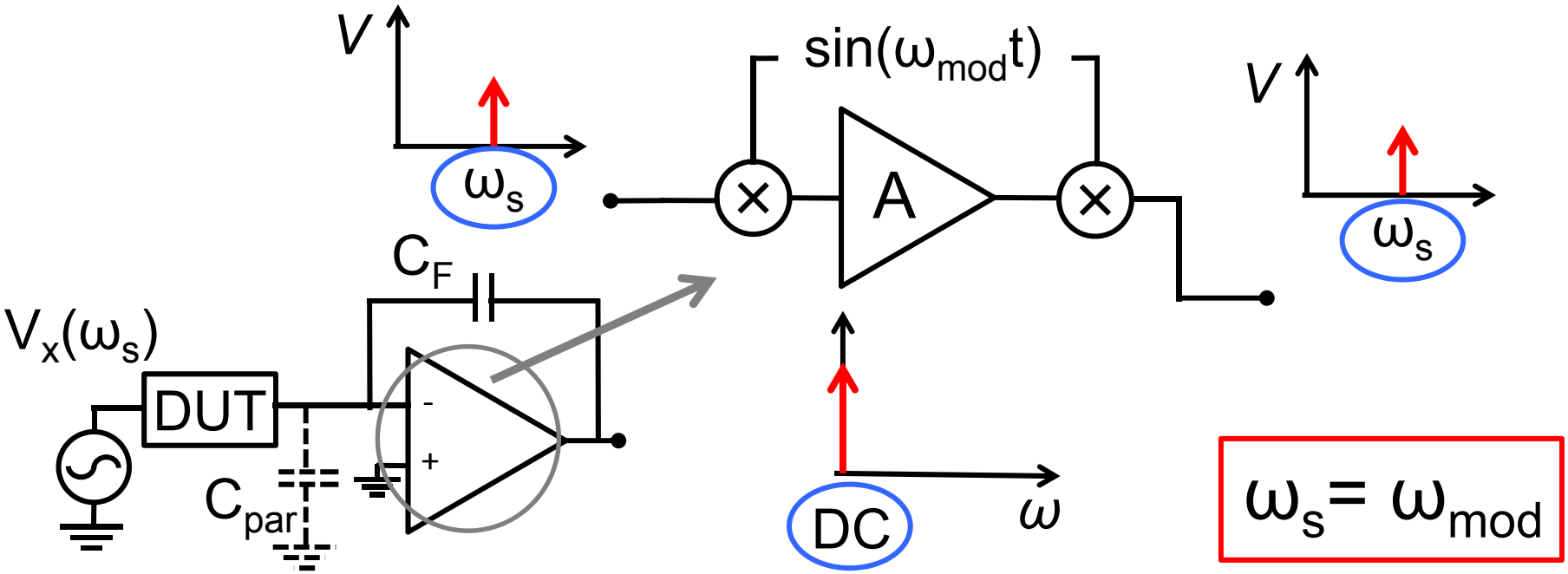


Standard Measurement Configuration



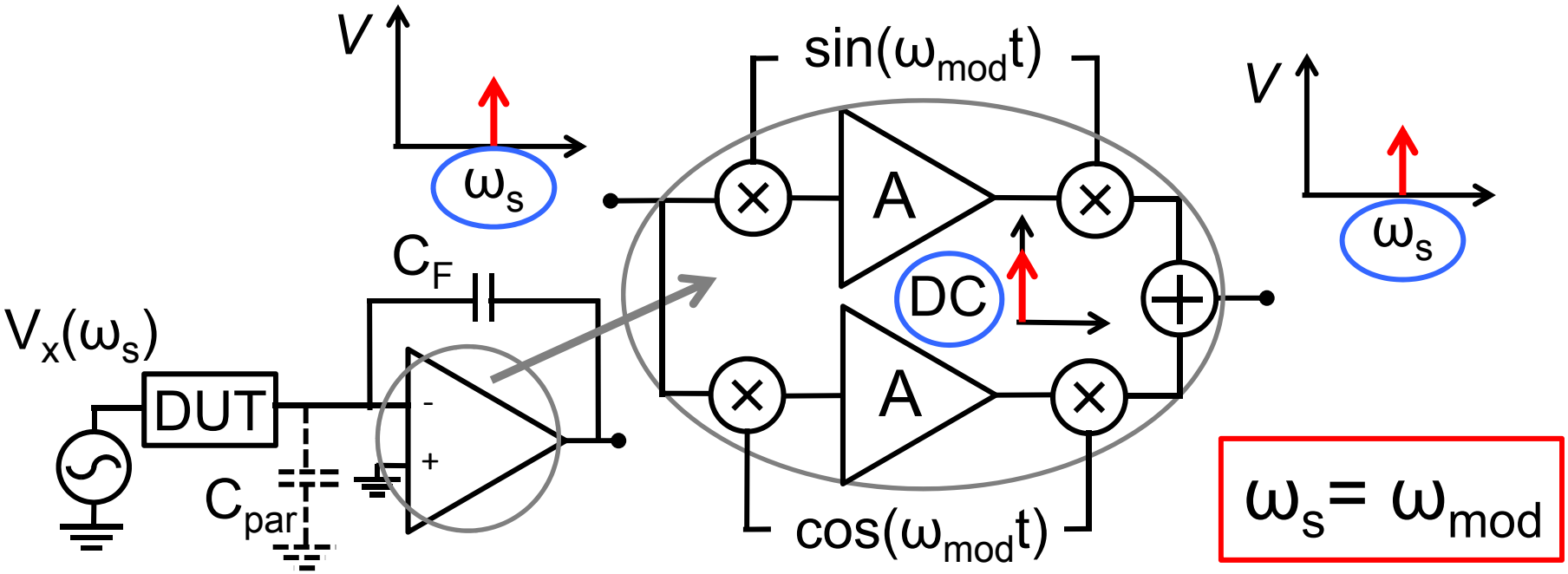
- Noise limit due to feedback resistor
- Bandwidth is determined by the external (and variable) C_{par}
- Poor Loop Gain, thus accuracy, for high frequency measurements

Proposed Configuration



- C_F feedback capacitance
- Signal translation for amplification
- High Loop Gain regardless of C_{par}

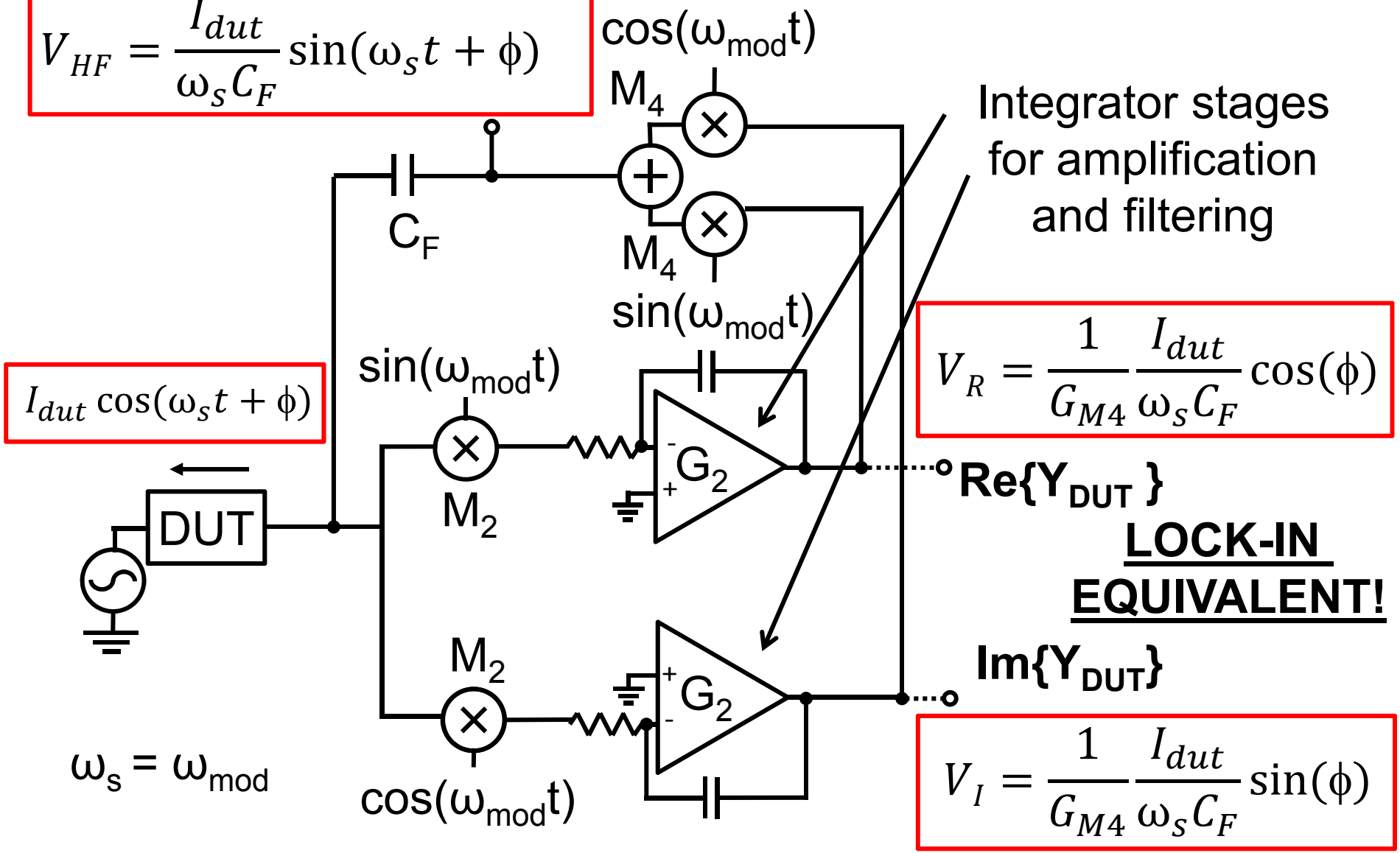
Proposed Configuration



- C_F feedback capacitance
- Signal translation for amplification
- High Loop Gain regardless of C_{par}

Feedback with Embedded Lock-in

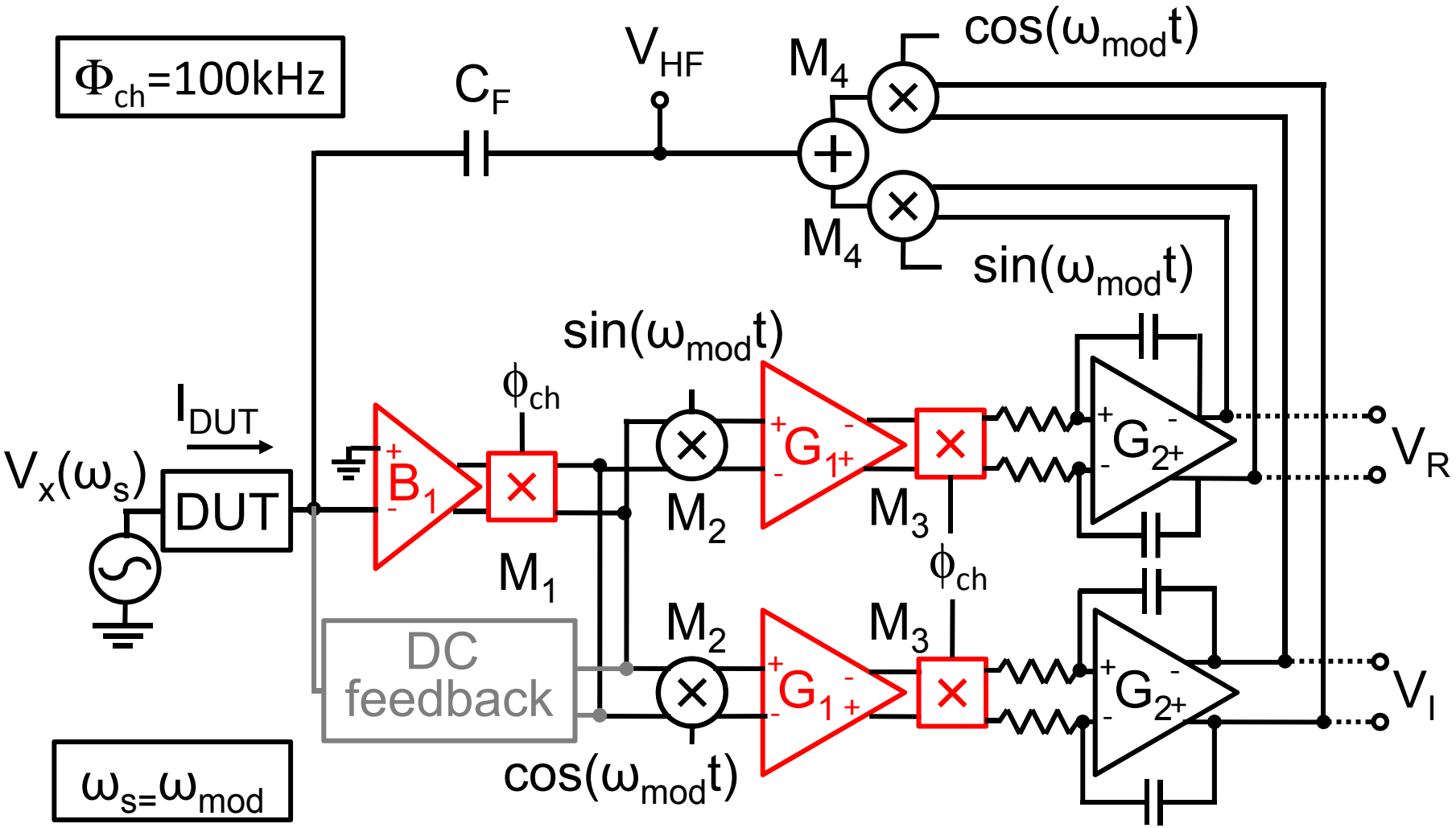
$$V_{HF} = \frac{I_{dut}}{\omega_s C_F} \sin(\omega_s t + \phi)$$



$$V_R = \frac{1}{G_{M4}} \frac{I_{dut}}{\omega_s C_F} \cos(\phi)$$

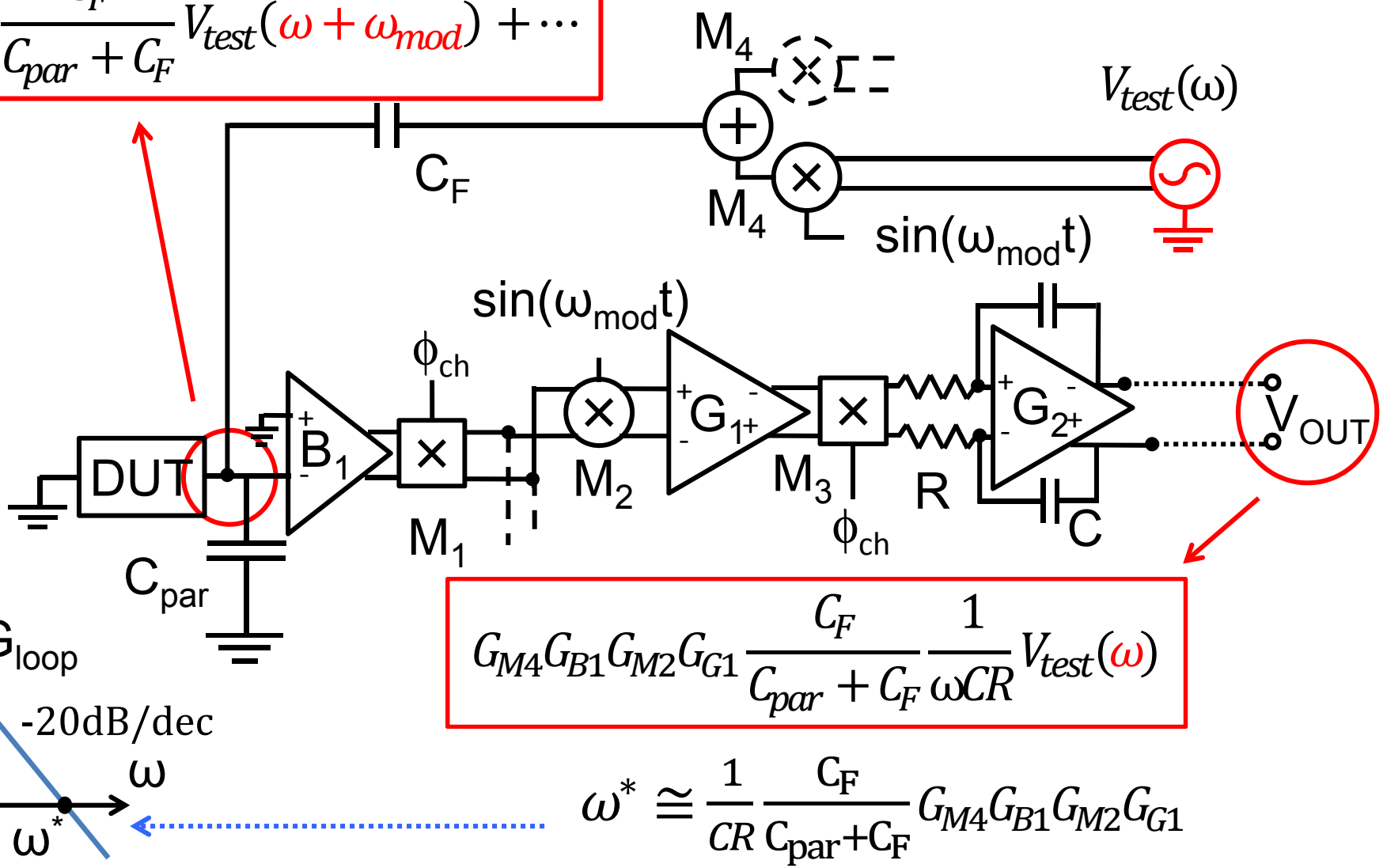
$$V_I = \frac{1}{G_{M4}} \frac{I_{dut}}{\omega_s C_F} \sin(\phi)$$

Feedback Complete Architecture



Feedback Loop Gain

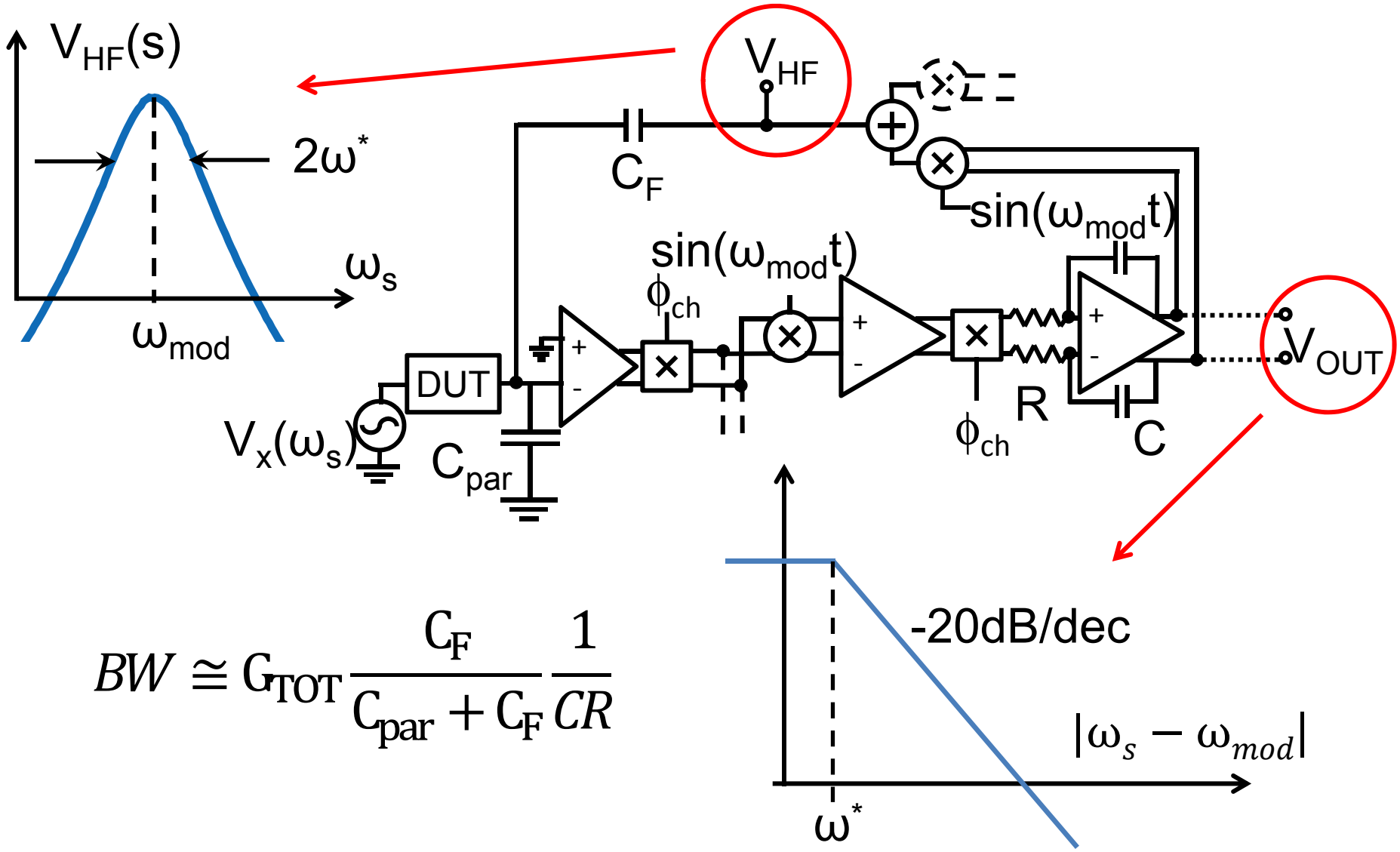
$$G_{M4}\frac{C_F}{C_{par}+C_F}V_{test}(\omega+\omega_{mod})+\cdots$$



$$G_{M4}G_{B1}G_{M2}G_{G1}\frac{C_F}{C_{par}+C_F}\frac{1}{\omega CR}V_{test}(\omega)$$

$$\omega^* \cong \frac{1}{CR}\frac{C_F}{C_{par}+C_F}G_{M4}G_{B1}G_{M2}G_{G1}$$

Closed Loop Bandwidth

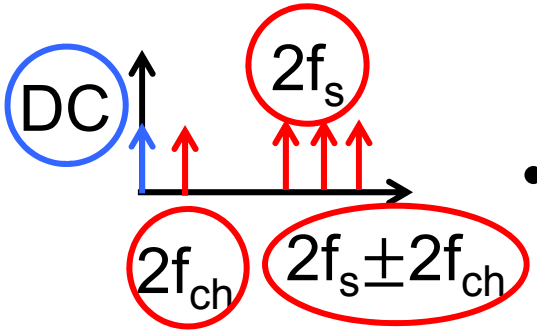


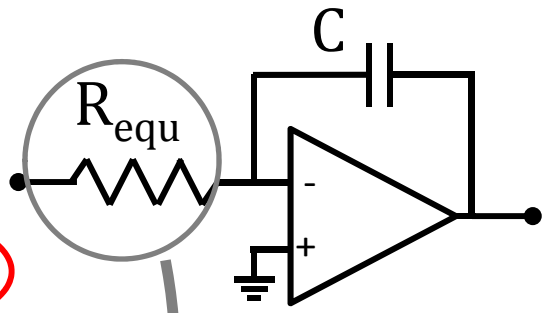
$$BW \cong G_{TOT} \frac{C_F}{C_{par} + C_F} \frac{1}{CR}$$

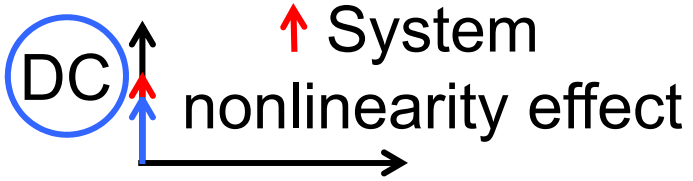
Integrator Filter Specifications

$1\ \text{aF resolution} \rightarrow BW \approx 10Hz \longrightarrow C = 1.6\text{pF}$

$\boldsymbol{R_{equ} = 10\text{G}\Omega}$

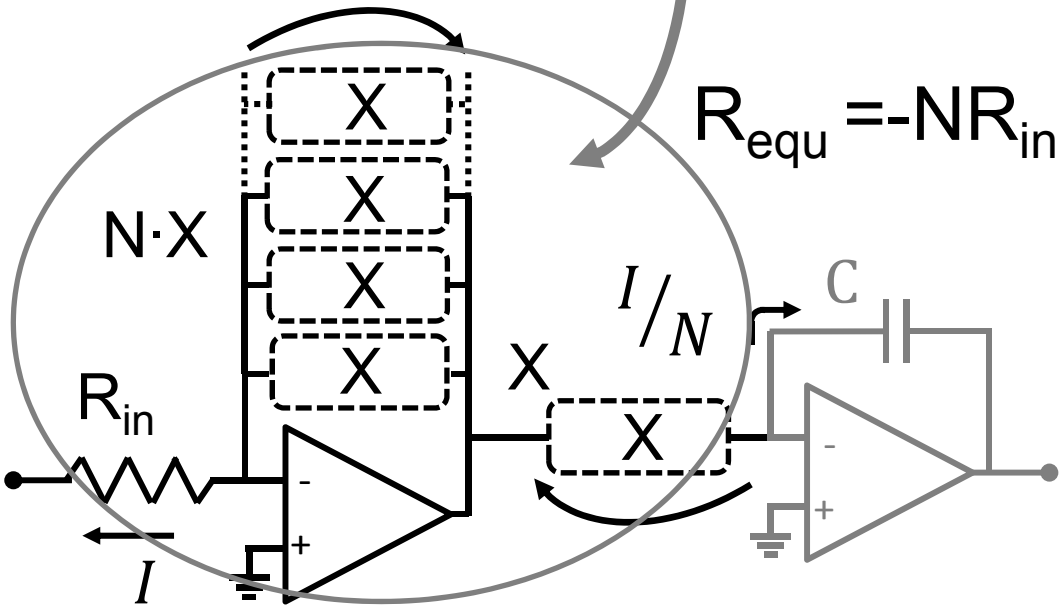




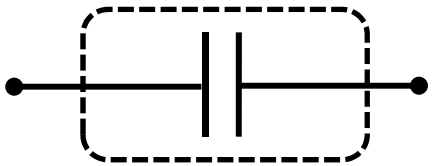


10GΩ active resistance: CURRENT DIVIDER

$R_{equ} = -NR_{in}$



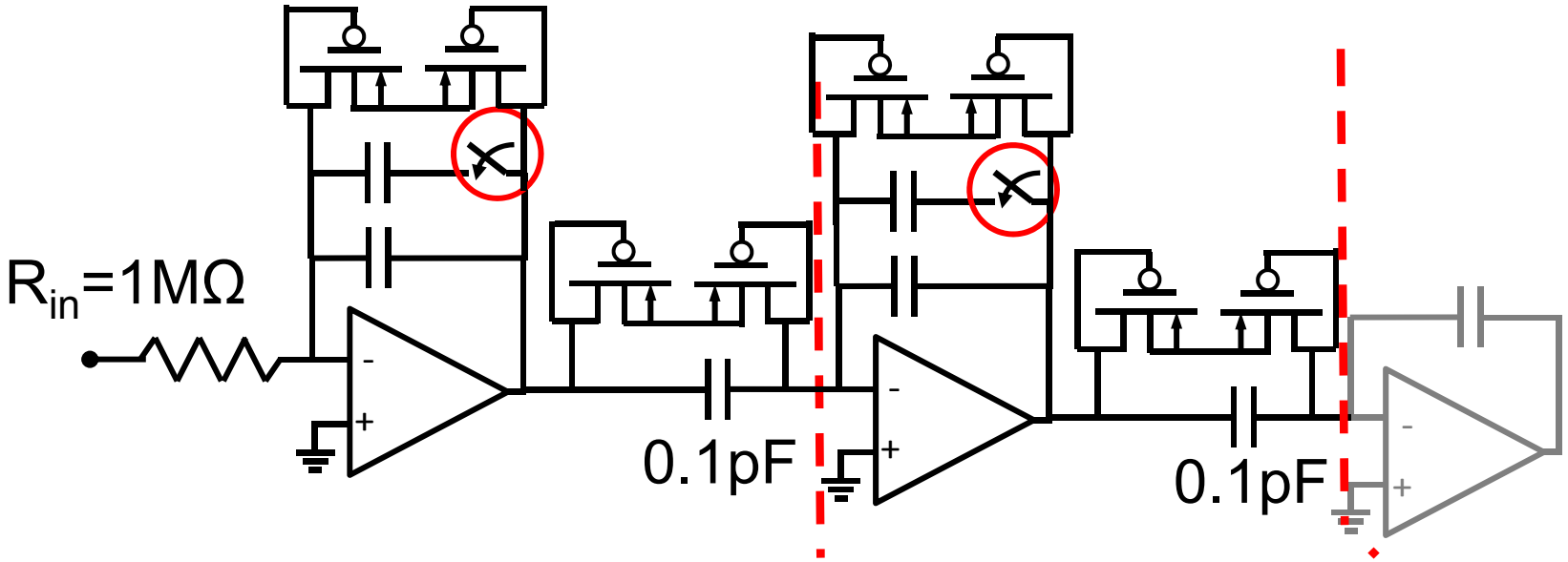
"X" to be chosen for highly linear characteristic



Integrator Filter Topology

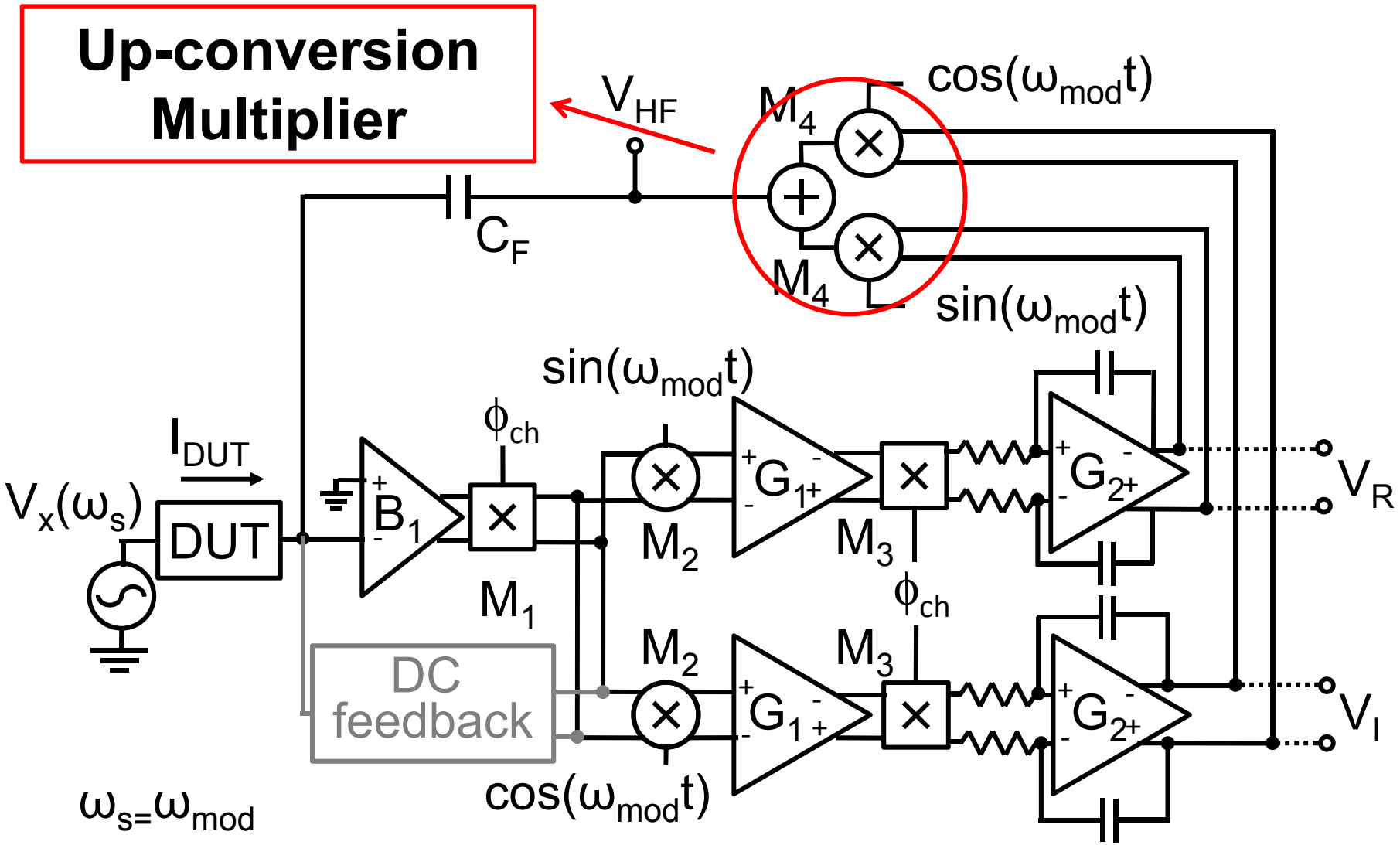
DC path:

- Symmetric → Low Nonlinear contribution
- Off in steady state conditions

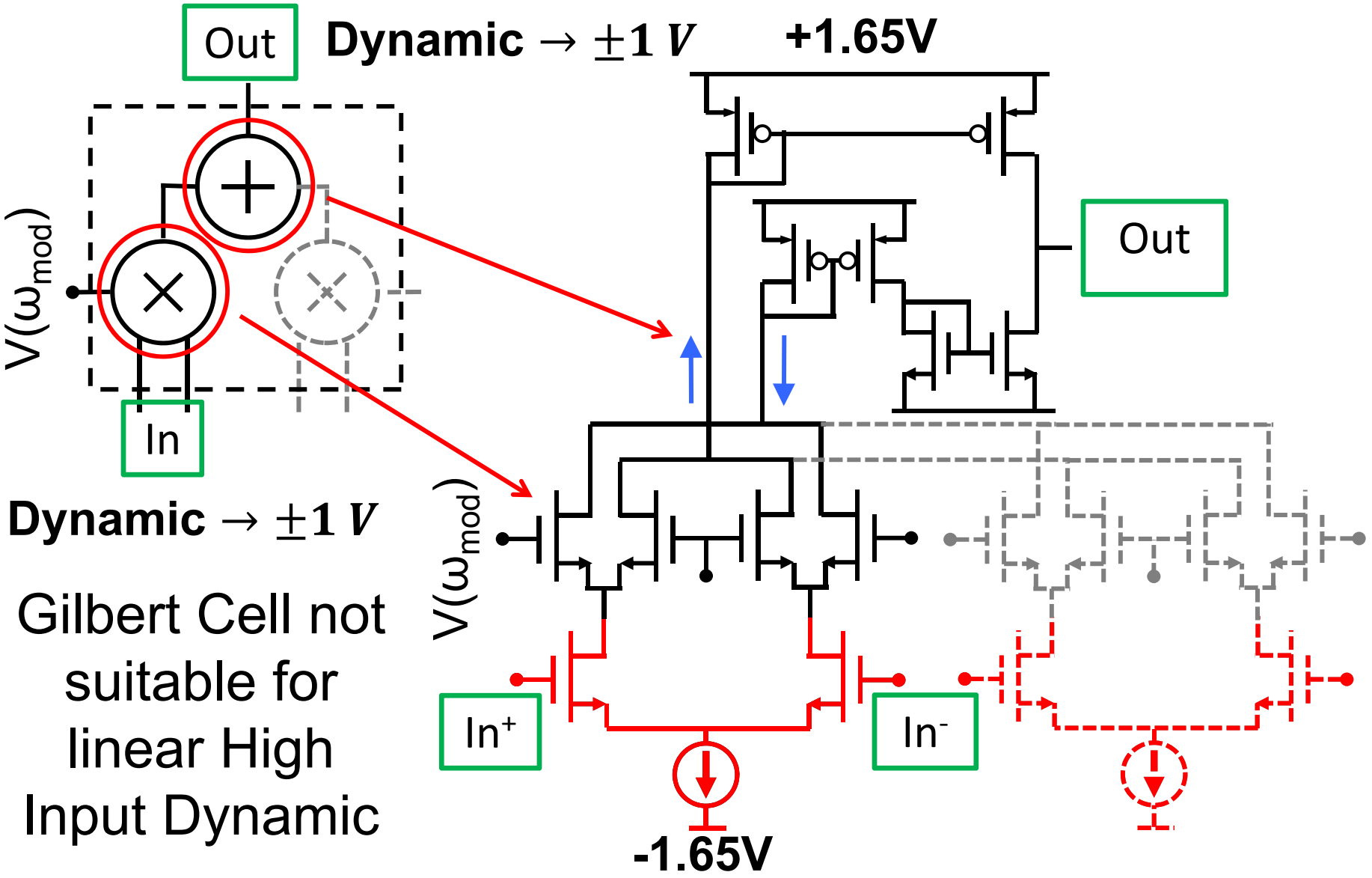


ATT_1, ATT_2	5	100
2	10MΩ (10kHz)	200MΩ (500Hz)
100	500MΩ (200Hz)	10GΩ (10Hz)

Feedback Complete Architecture

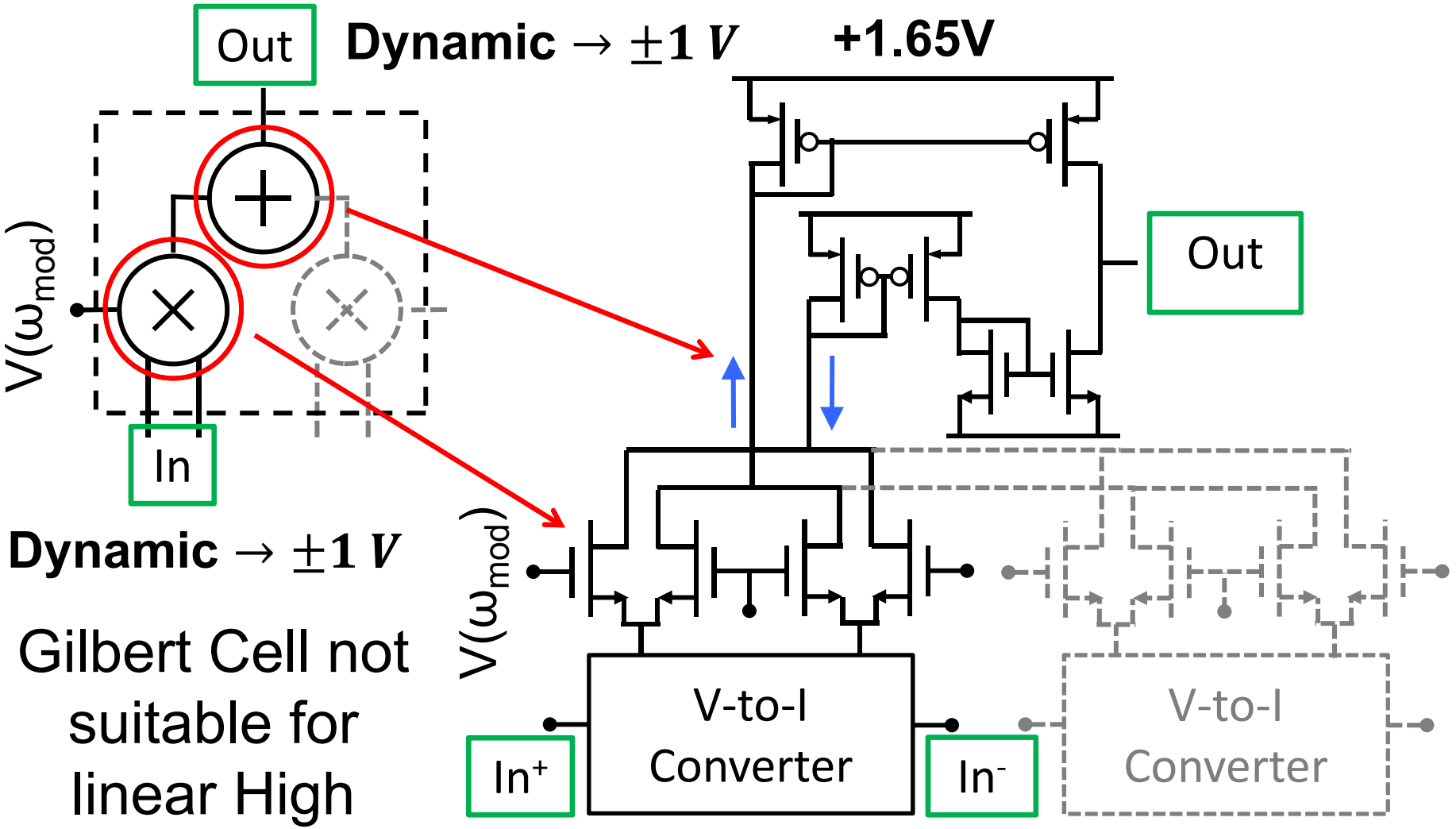


Up-conversion Multiplier



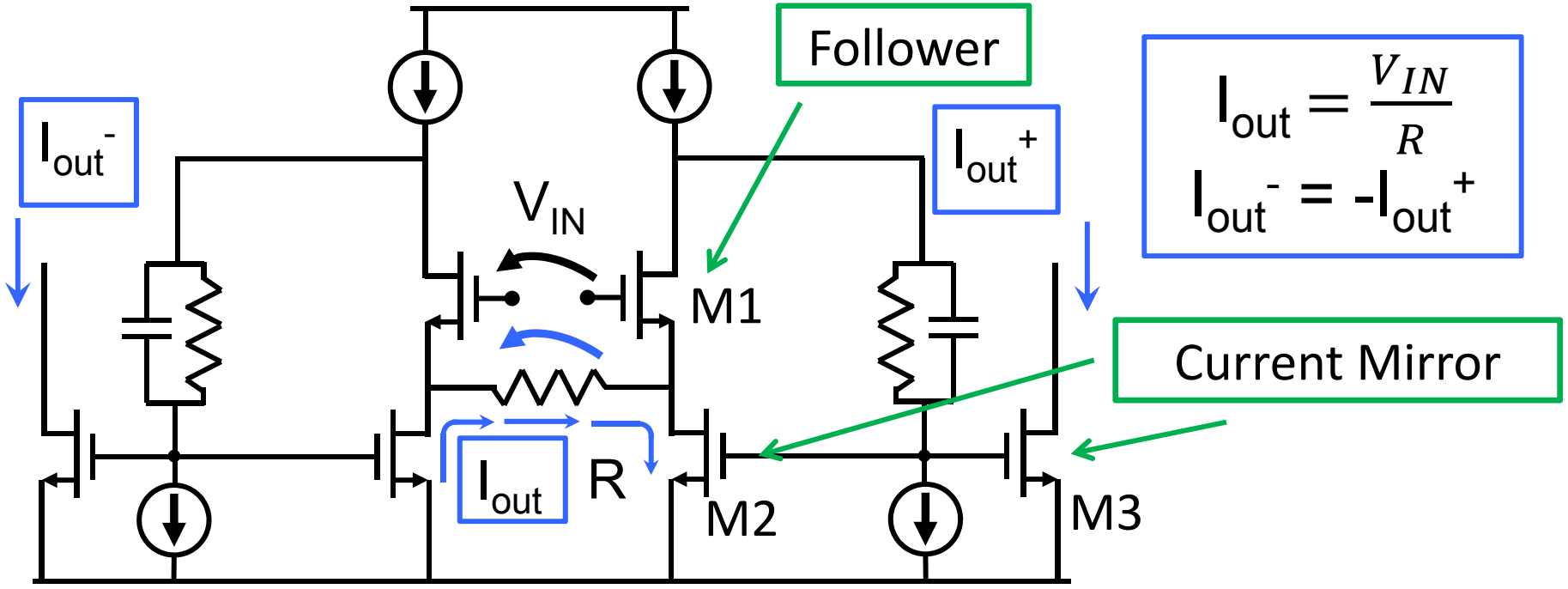
Gilbert Cell not suitable for linear High Input Dynamic

Up-conversion Multiplier



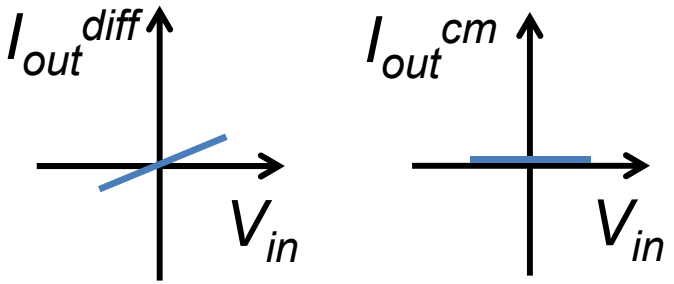
Gilbert Cell not suitable for linear High Input Dynamic

V-to-I Converter

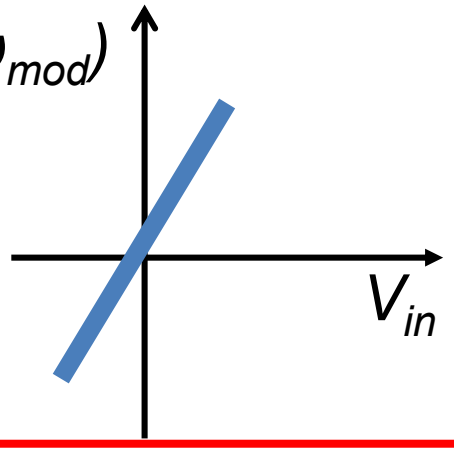


$$I_{out} = \frac{V_{IN}}{R}$$
$$I_{out}^- = -I_{out}^+$$

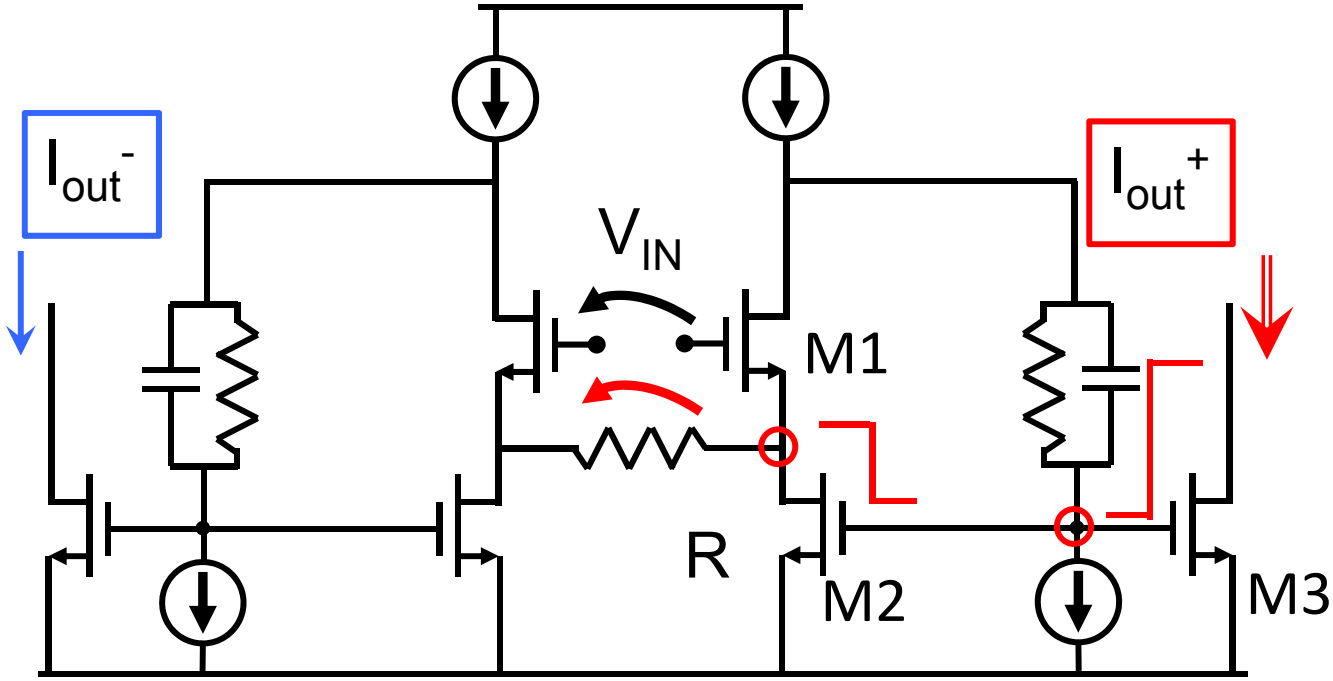
V-to-I Characteristic



Multiplier Conversion Gain



V-to-I Converter

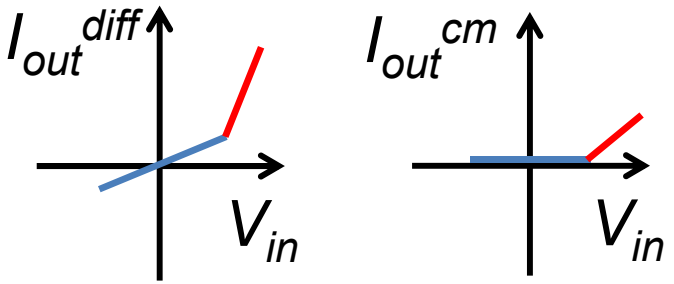


Non-monotonic characteristic

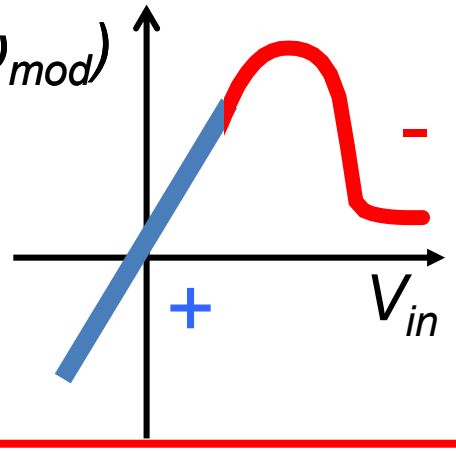
$G_{loop}(\omega) > 0$

Loop instability

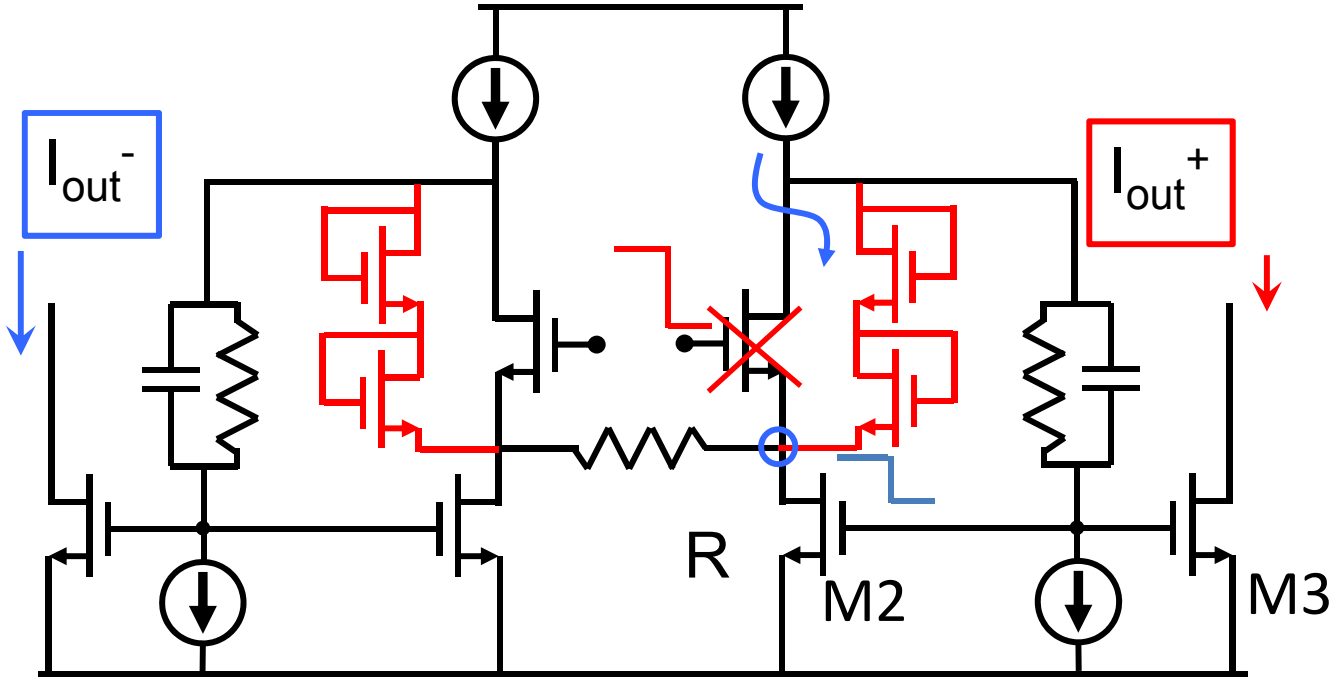
V-to-I Characteristic



Multiplier Conversion Gain



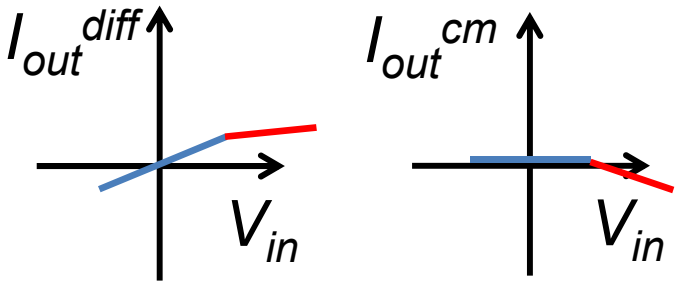
V-to-I Converter



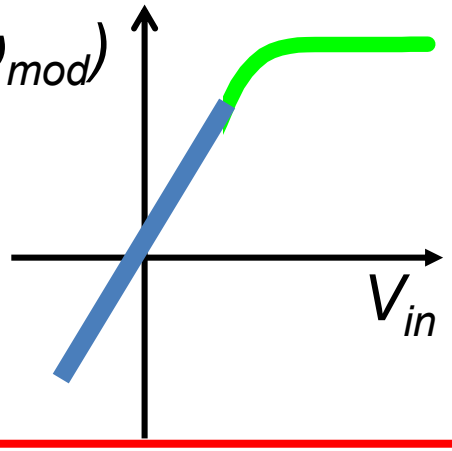
Monotonic characteristic

1% Linearity Error for $\Delta V_{IN} = \pm 1V$ (V_{dd} = 3.3V)

V-to-I Characteristic



Multiplier Conversion Gain

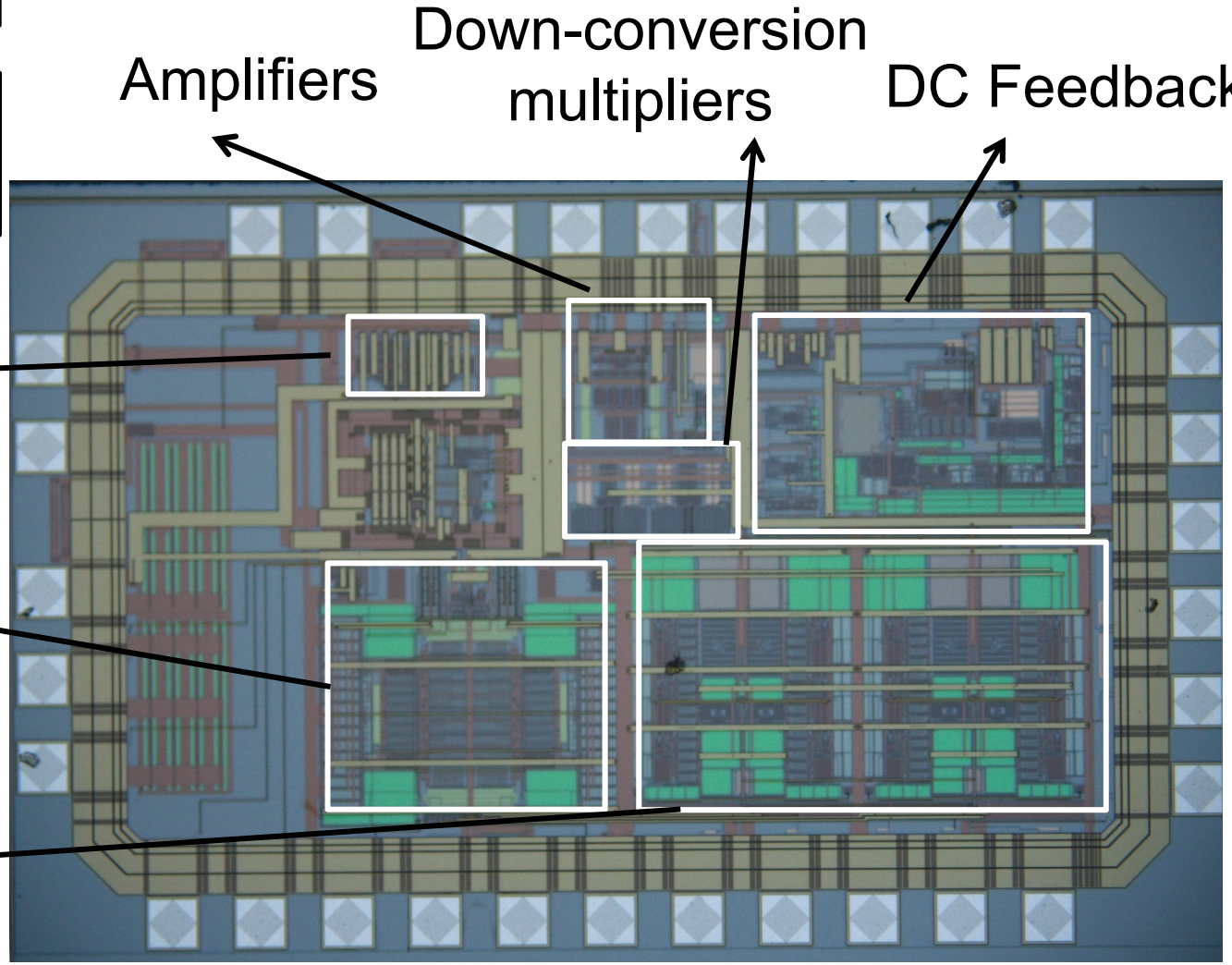


ASIC implementation

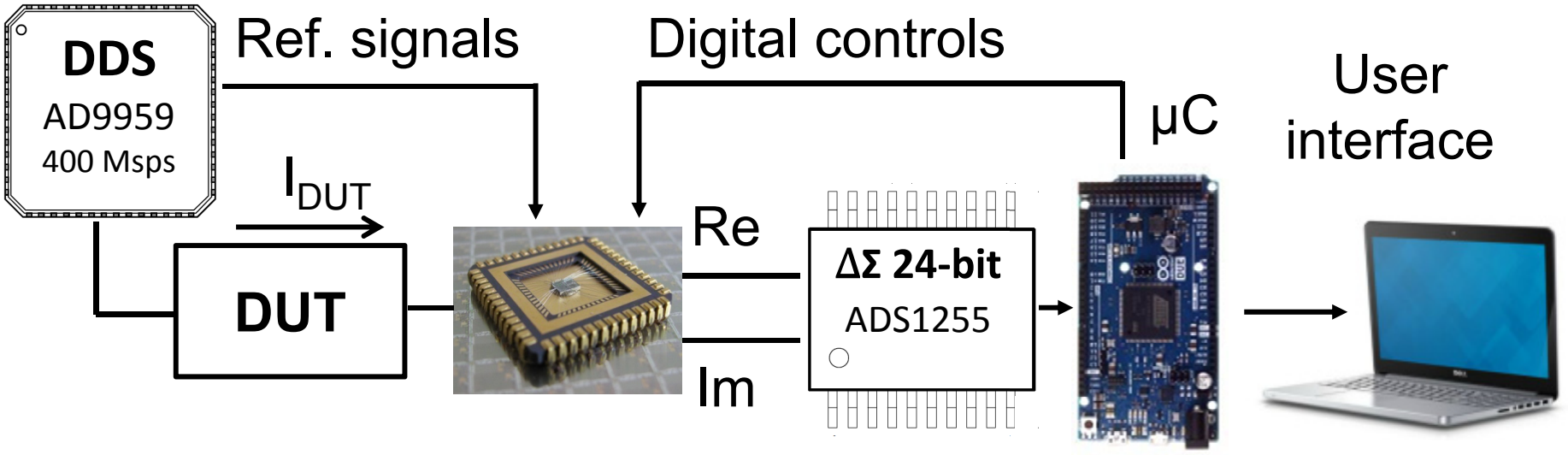
AMS 0.35µm technology

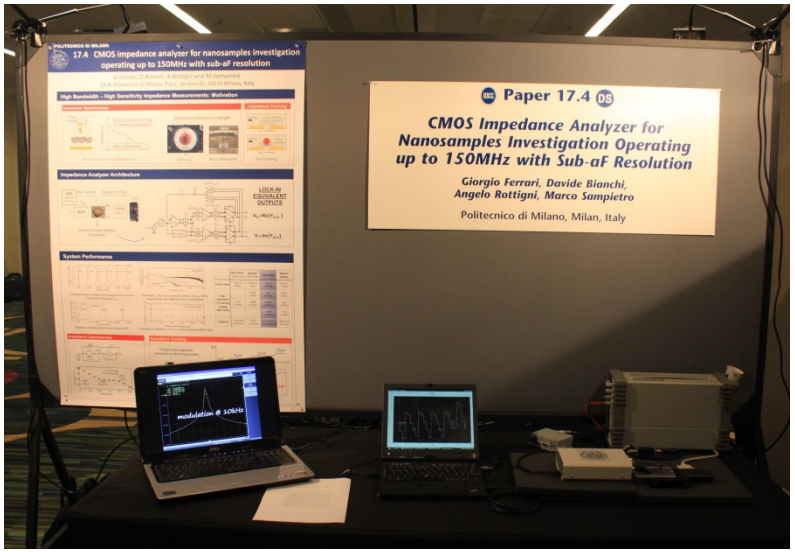
3.3V ; 45mA

1.3mm x 2mm die size

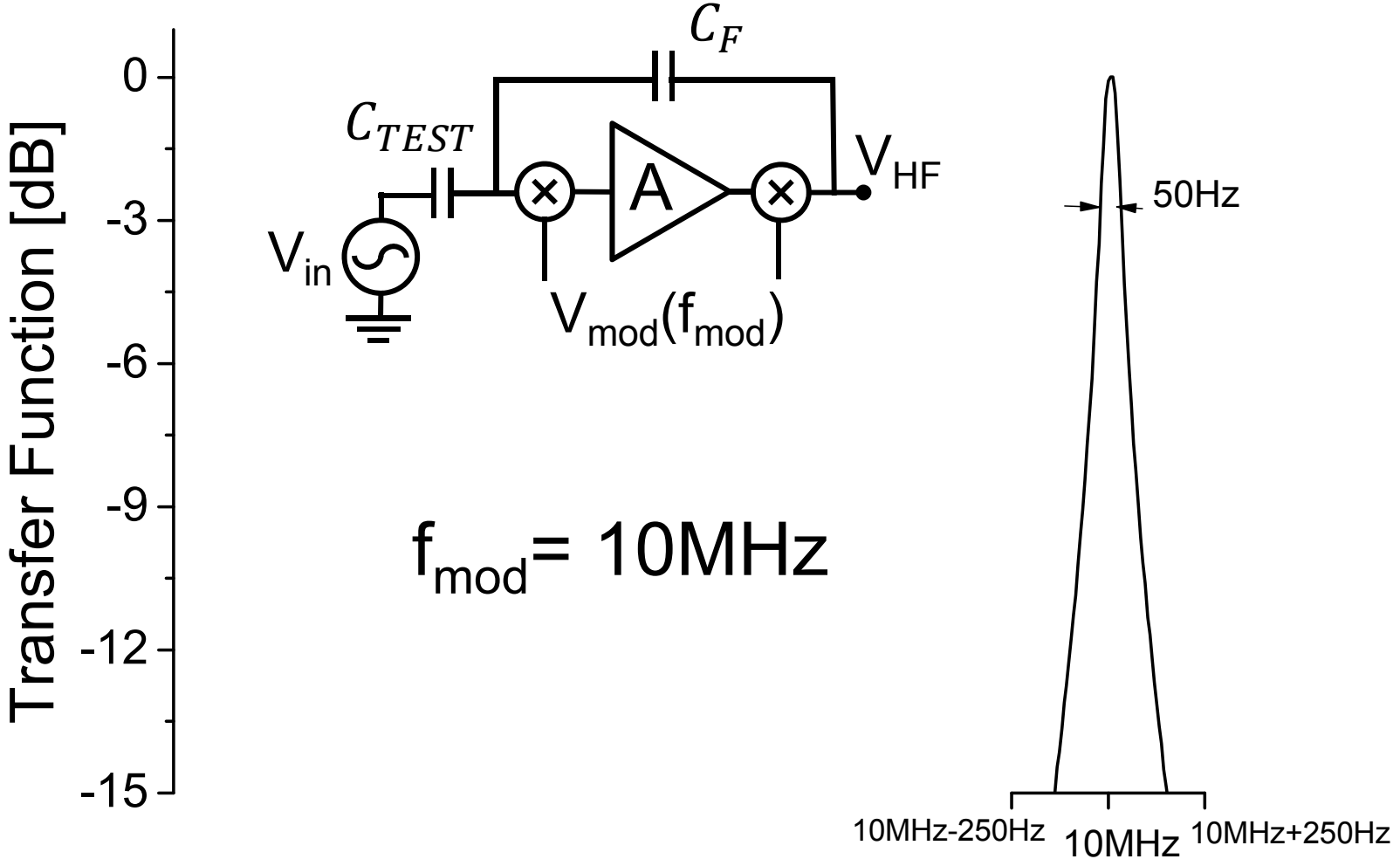


Impedance analyzer architecture

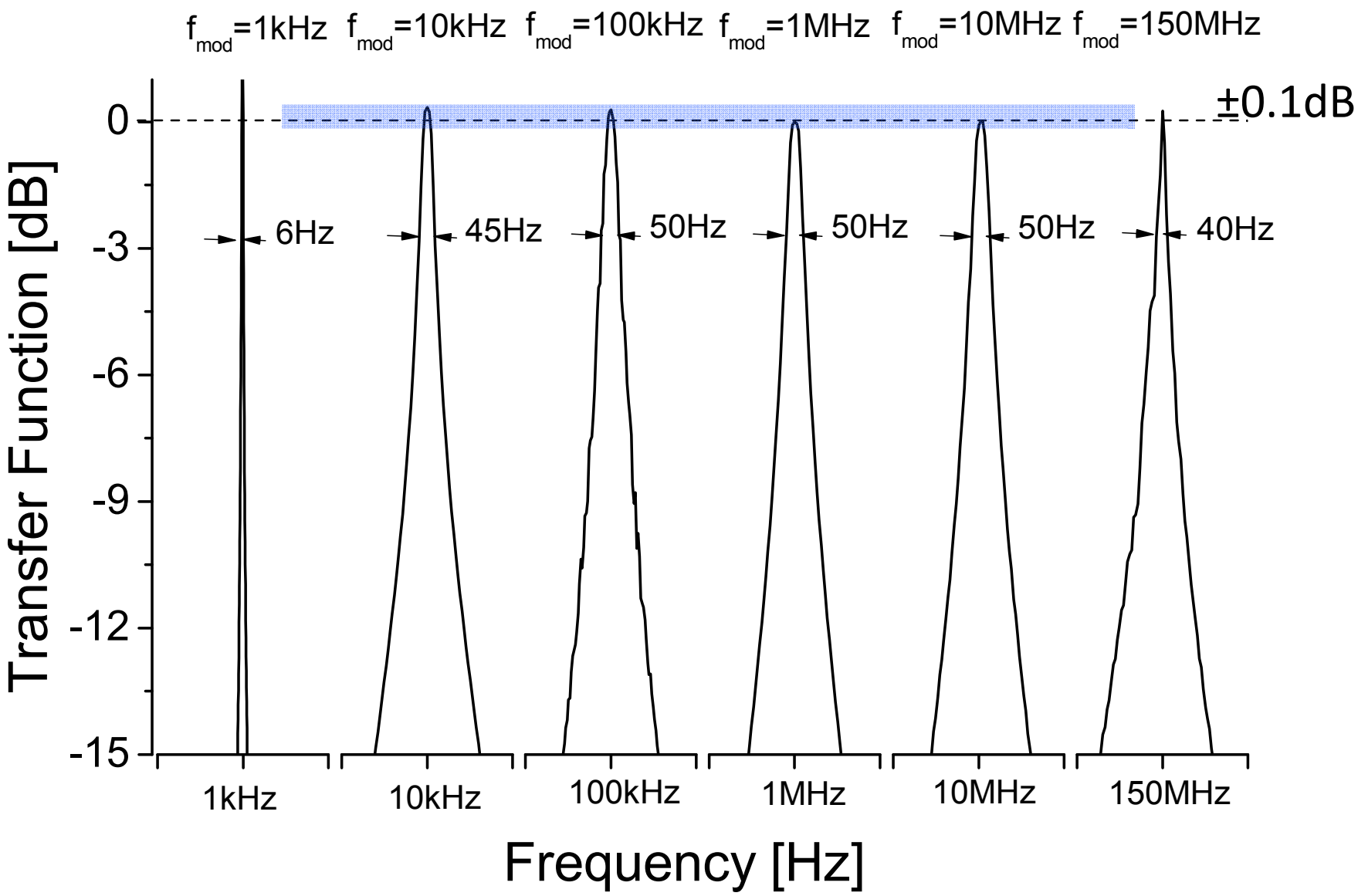




Exp. results: Transfer Function

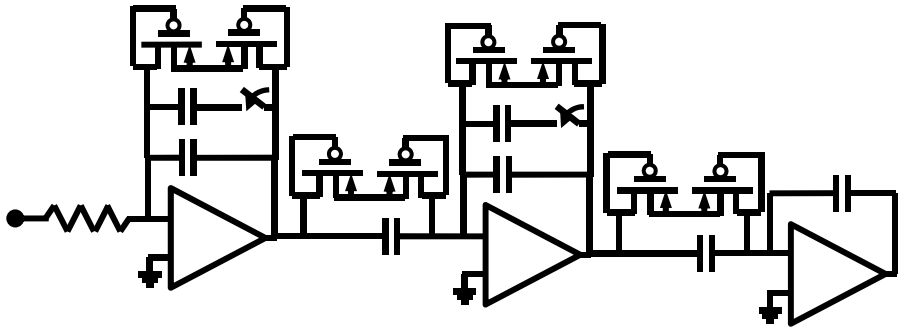


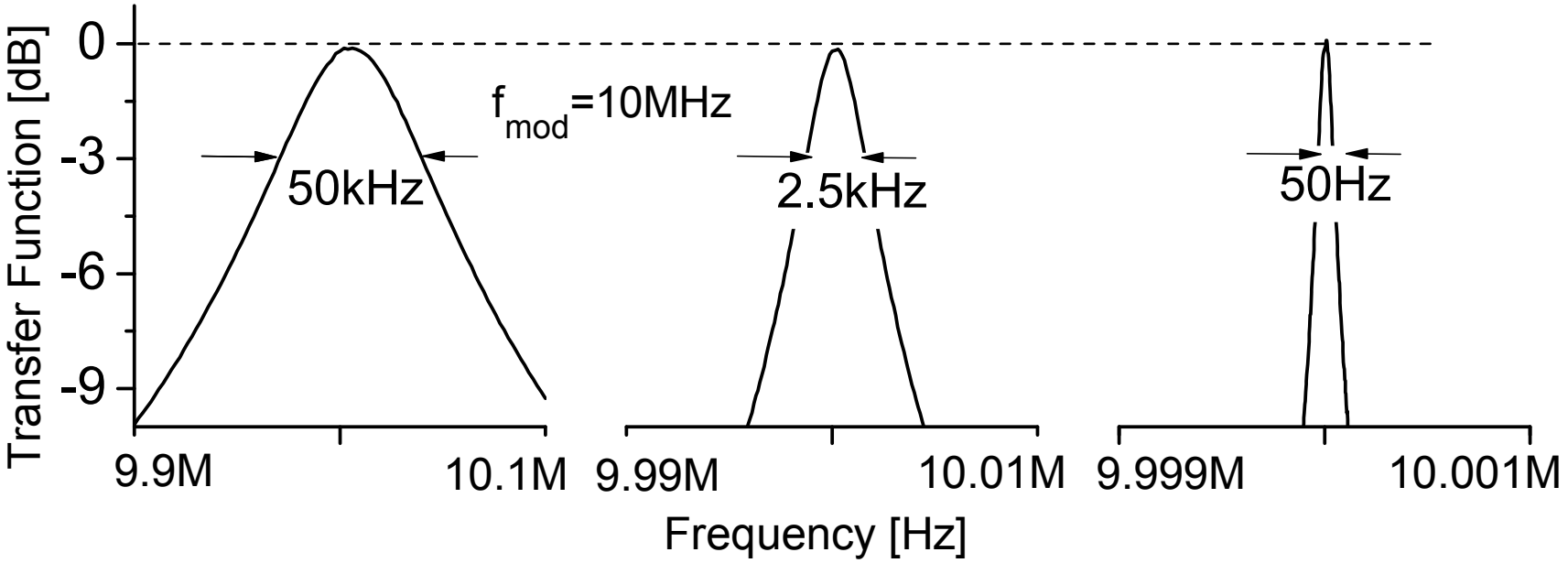
Exp. results: Transfer Function



Exp. Results: Selectable Bandwidth

INTEGRATOR FILTER



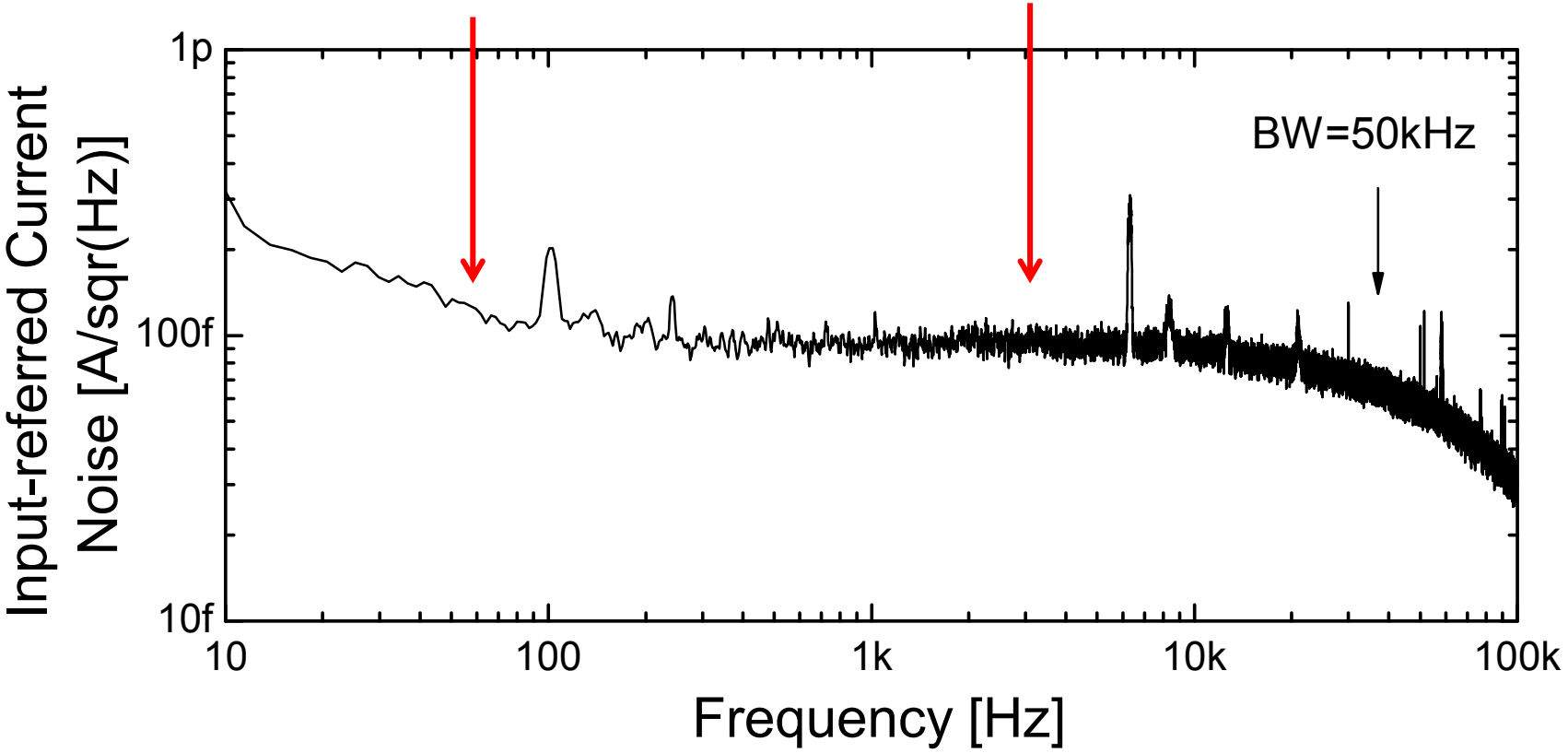


$R_{EQ} = 10M\Omega$ $R_{EQ} = 200M\Omega$ $R_{EQ} = 10G\Omega$

Exp. Results: Input Current Noise

Corner Frequency → $60Hz$

White noise → $100\,fA/\sqrt{Hz}$

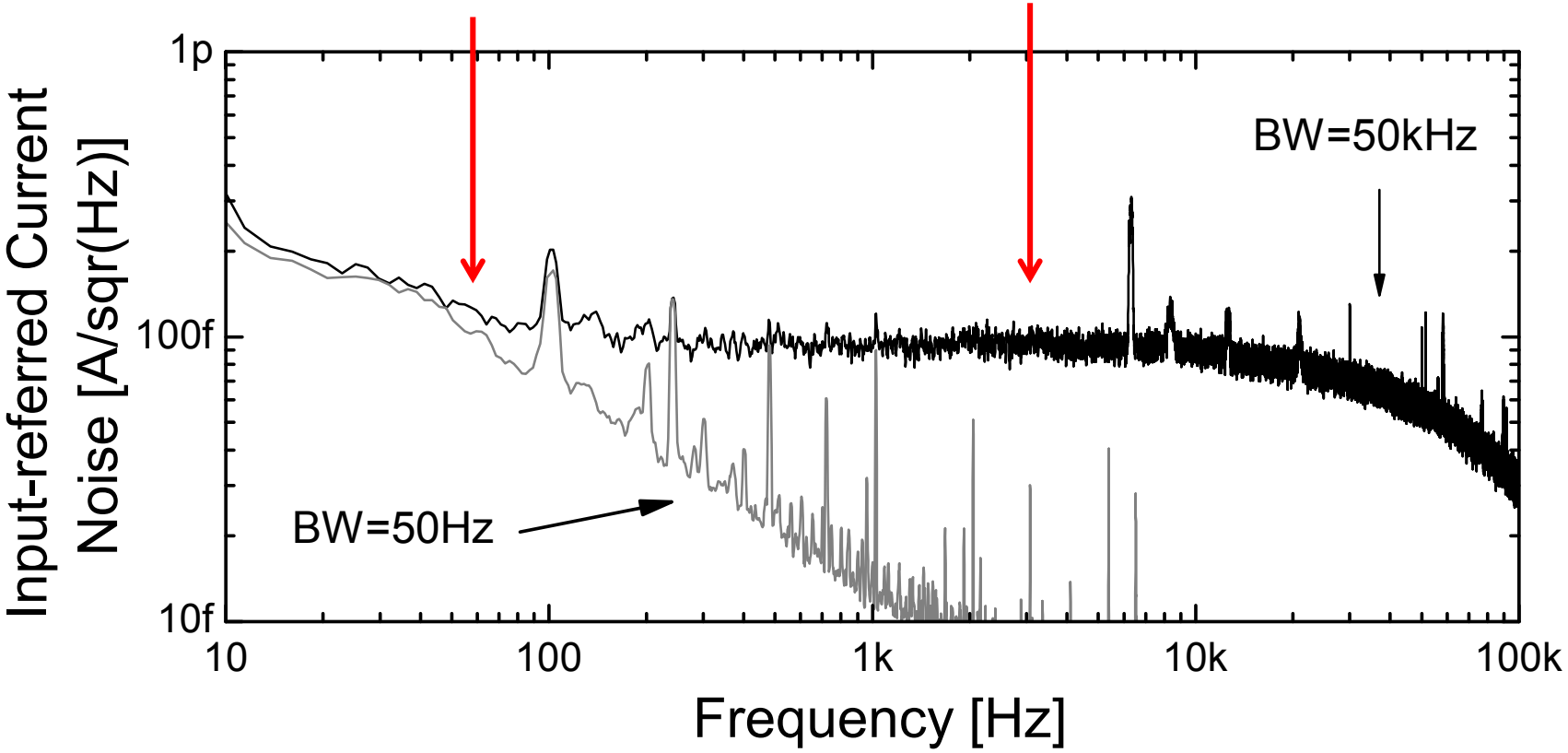


Equivalent input noise spectral density at f_{mod}=1MHz

Exp. Results: Input Current Noise

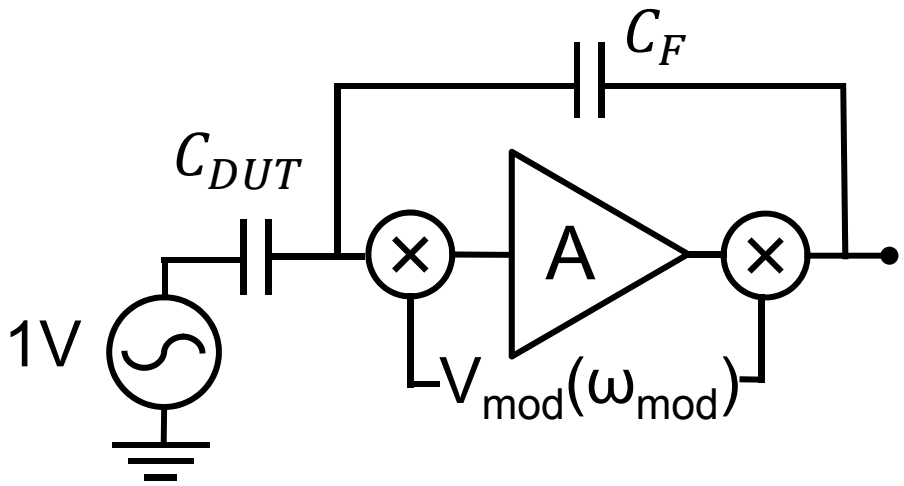
Corner Frequency → $60Hz$

White noise → $100\,fA/\sqrt{Hz}$

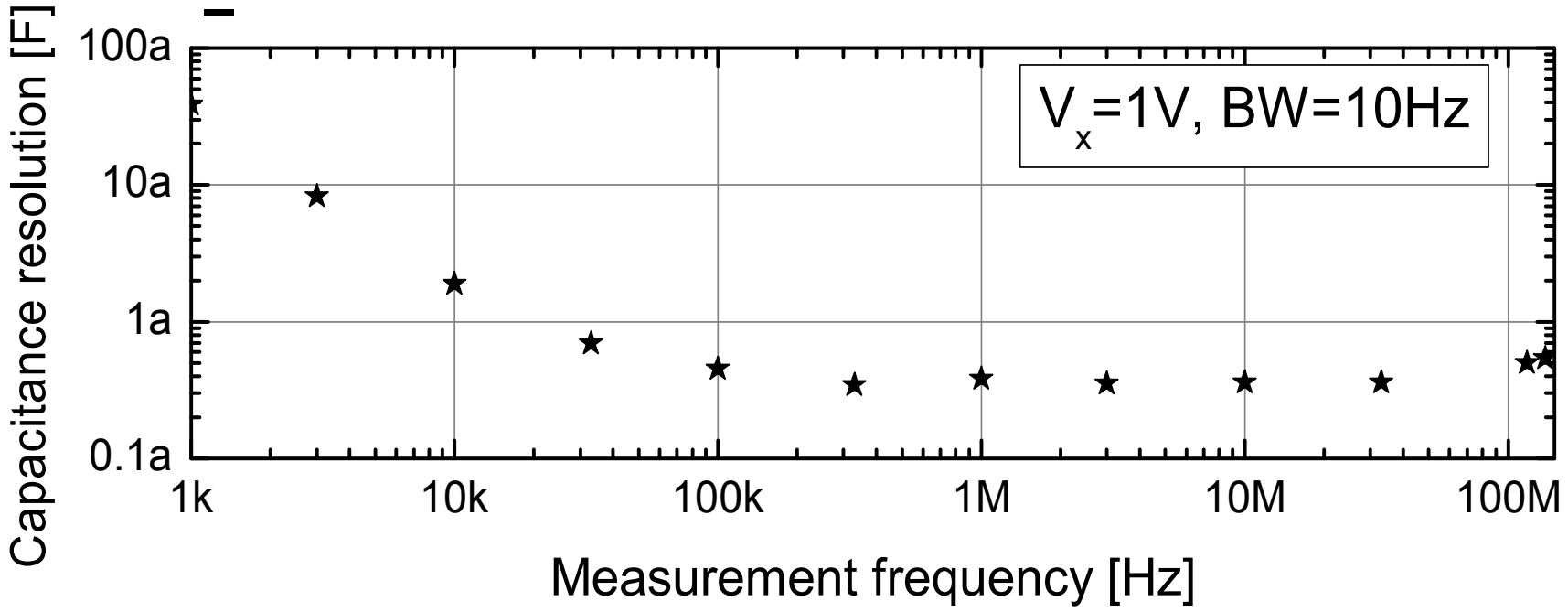


Equivalent input noise spectral density at f_{mod}=1MHz measured for two different lock-in BW

Exp. Results: Impedance Resolution

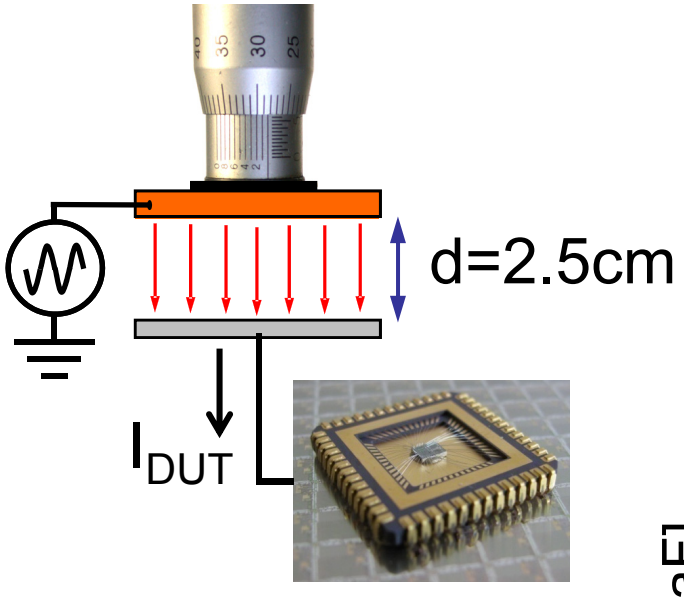


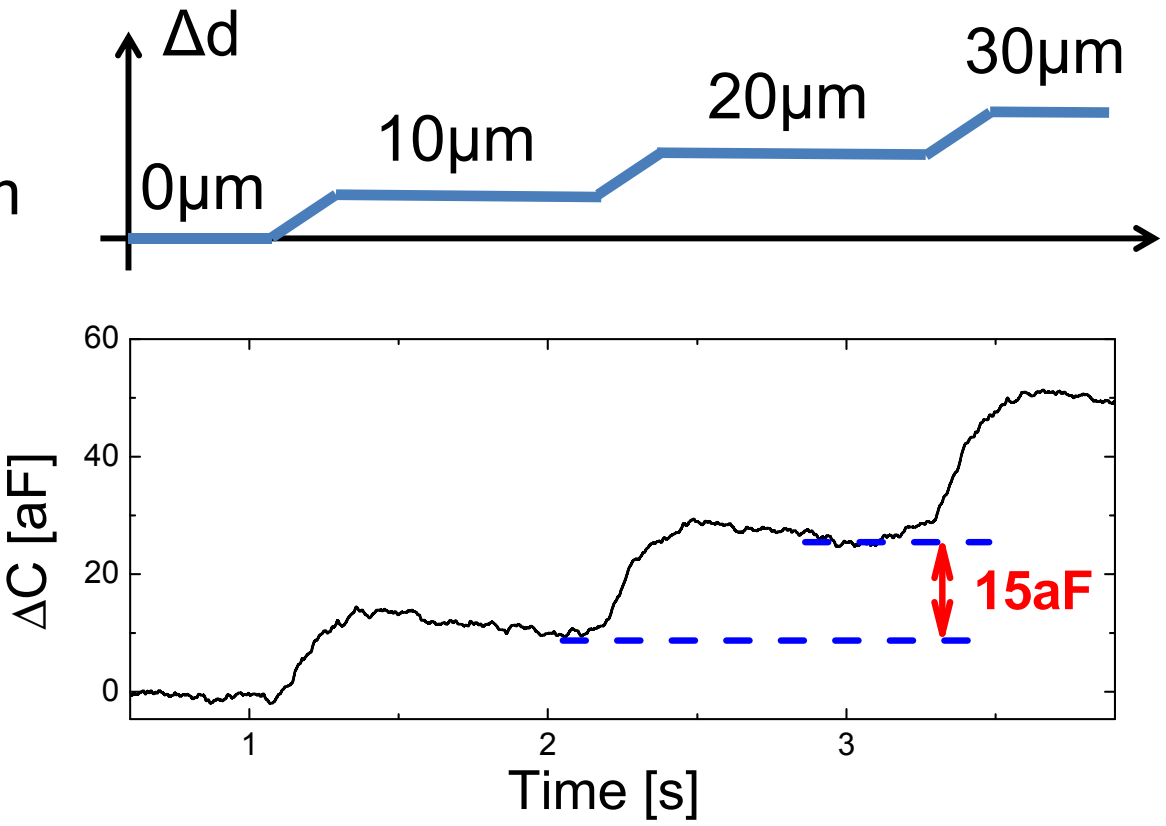
Attofarad resolution
from 20kHz to 150MHz



Exp. Results: Impedance Time-tracking

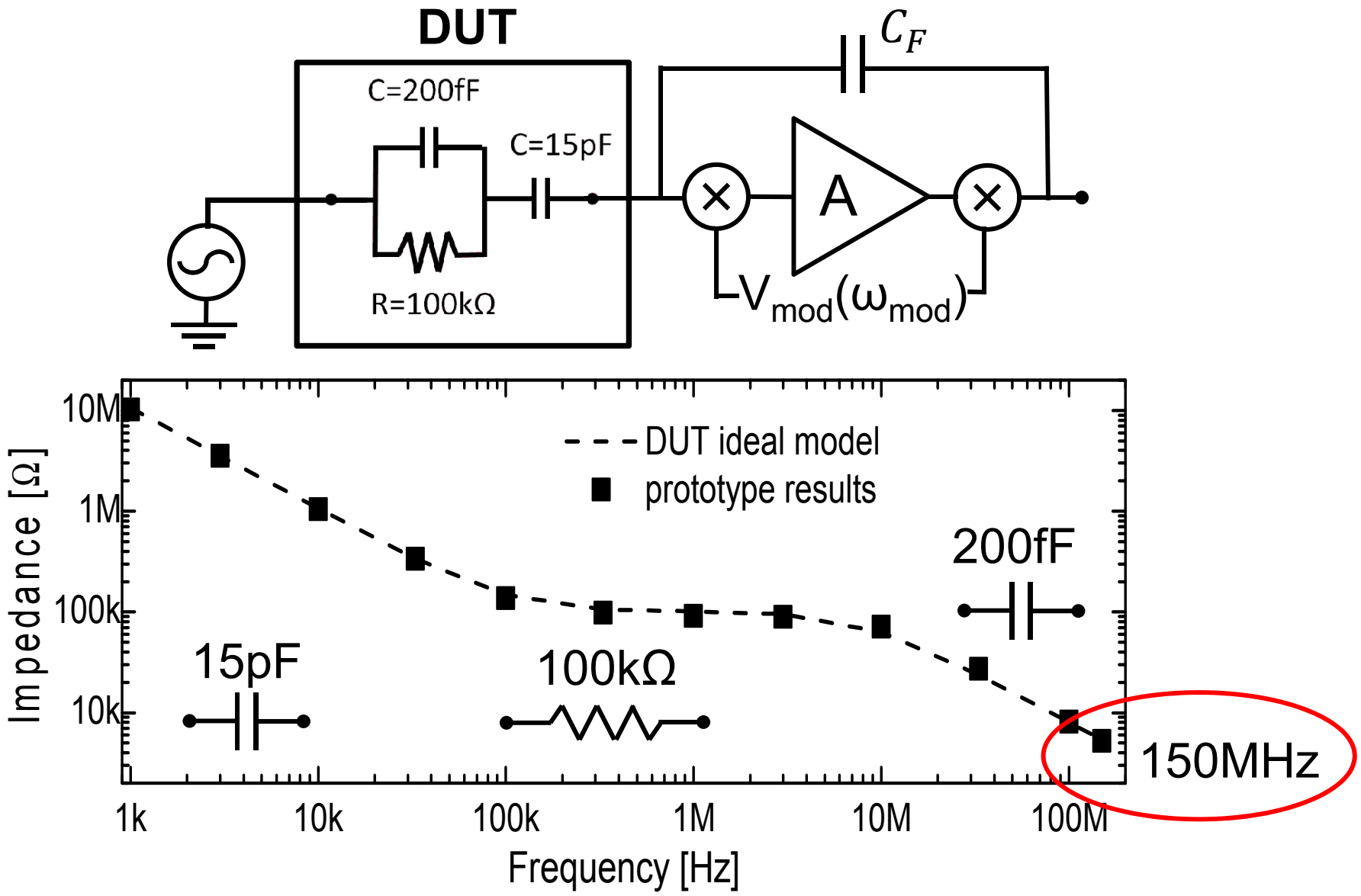
Parallel-plate capacitor controlled by Micromanipulator





$$\Delta C = C \cdot \frac{\Delta d}{d}$$

Exp. Results: Impedance Spectroscopy



Exp. Result: Performance Comparison

	Manickam ISSCC 2010	**Gozzini** ISSCC 2009	**This work**	**Agilent 4294A**
Freq. range	10Hz to 50MHz	100Hz to 2MHz	1kHz to 150MHz	40Hz to 110MHz
Cap. resolution (1V exciting voltage, BW=10Hz)	-	0.25aF (10kHz)	2aF (10kHz)	250aF (10kHz)
	6.4aF (2.5MHz)	0.05aF (2.5MHz)	0.35aF (2.5MHz)	8aF (2.5MHz)
			0.6aF (150MHz)	11aF (110MHz)
Features	Low-power Multichannel	High-Sensitivity	High-Sensitivity High-Bandwidth	Bench-top Instrument

Summary

Chip performing impedance spectroscopy and tracking:

- Dem/Mo structure for >100MHz spectroscopy
- Impedance information (Re, Im) directly available at DC on output pins
- 1kHz to 150MHz frequency range
- 1aF resolution (20kHz to 150MHz)
- Digitally selectable tracking from 20us to 100ms

Acknowledgment

Staff

Marco Sampietro
Giorgio Ferrari
Dario Natali

Master Students

Giorgio Infante
Cecilia Gatti
Emanuele Moretti
Andrea Palamara

Postdocs and PhDs

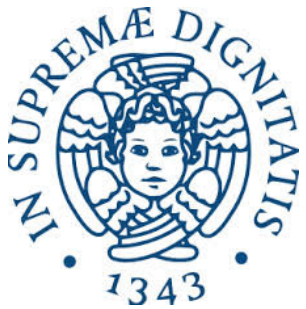
Marco Carminati
Maddalena Binda
Angelo Rottigni
Davide Bianchi
Giovanni Azzellino
Pietro Ciccarella
Giacomo Gervasoni

Thanks to Fondazione Cariplo, FP7-EU, Regione Lombardia

A 0.07 mm² 2-Channel Instrumentation Amplifier with 0.1% Gain Matching in 0.16µm CMOS

F. Sebastiano[1,2] , **F. Butti[3]**, R. van Veldhoven[1], P. Bruschi[4]

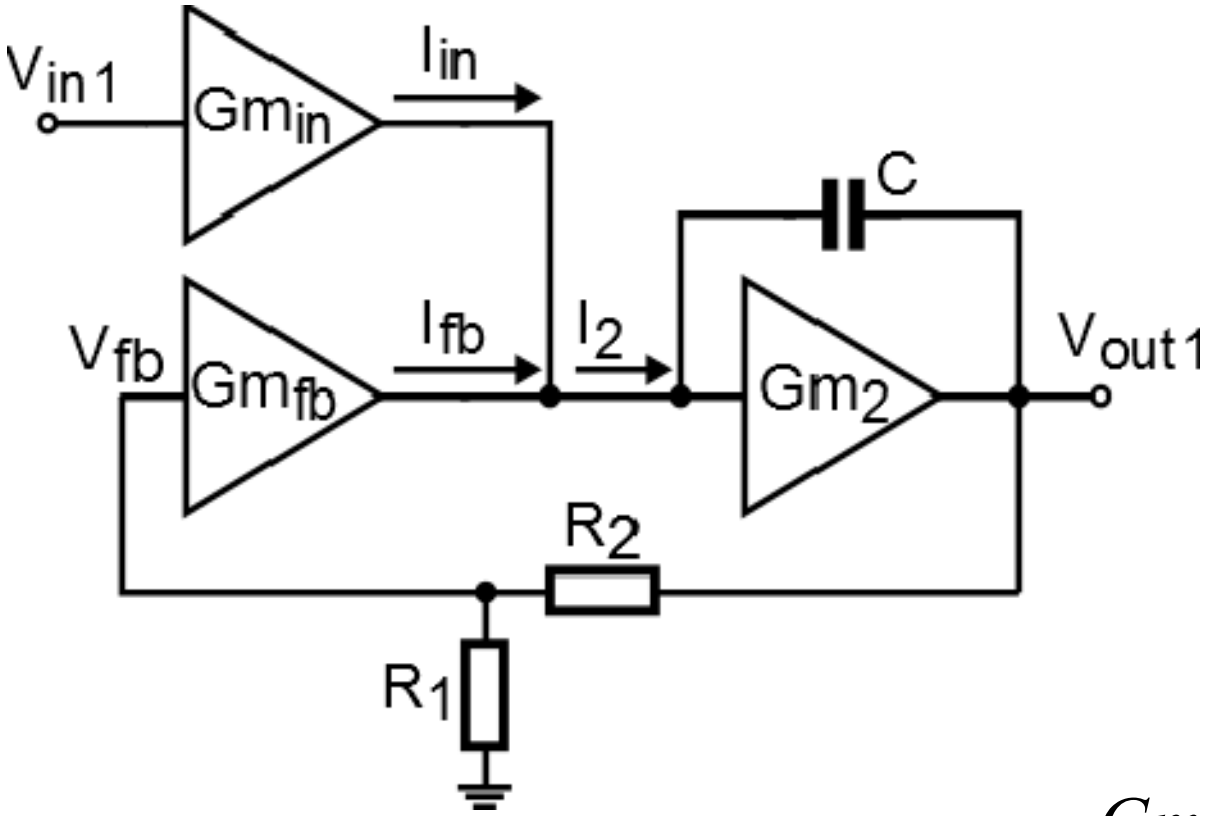
1. NXP Semiconductors, Eindhoven, The Netherlands
2. Delft University of Technology, Delft, The Netherlands
3. **University of Pisa, Italy, now with Marvell Italy**
4. University of Pisa



Introduction

- **Angular sensors for automotive applications:**
  - 2x magnetic sensors usually adopted
    - one output ∝ cos(α)
    - one output ∝ sin(α)
- Angle error < 0.1°: **gain mismatch < 0.15%**
- Signal bandwidth up to 20 kHz
- Resistive sensor bridges: high input impedance
- **Area < 0.1 mm²**

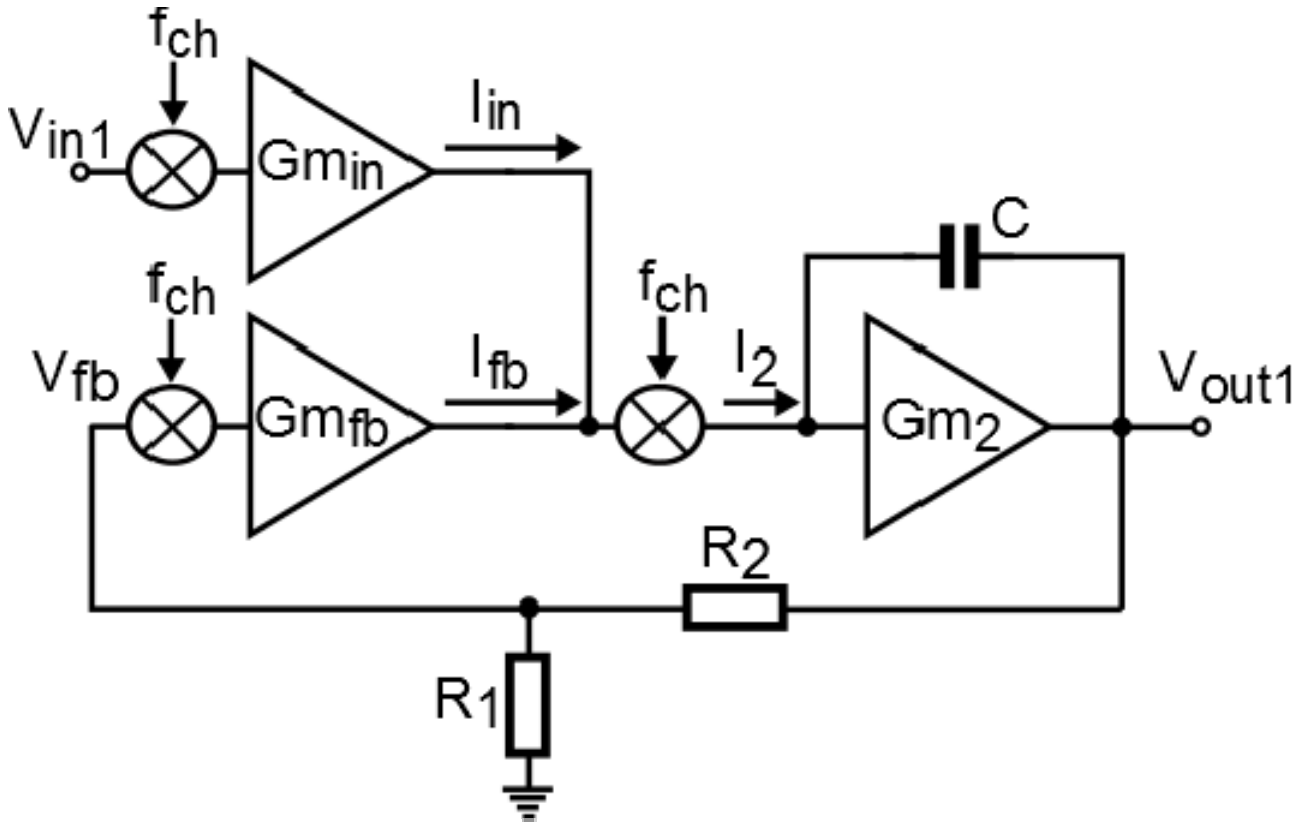
Single channel standard IA



- I_2 is nulled thanks to negative feedback: $$A = \frac{Gm_{in}}{Gm_{fb}} \cdot \left(1 + \frac{R_2}{R_1}\right)$$

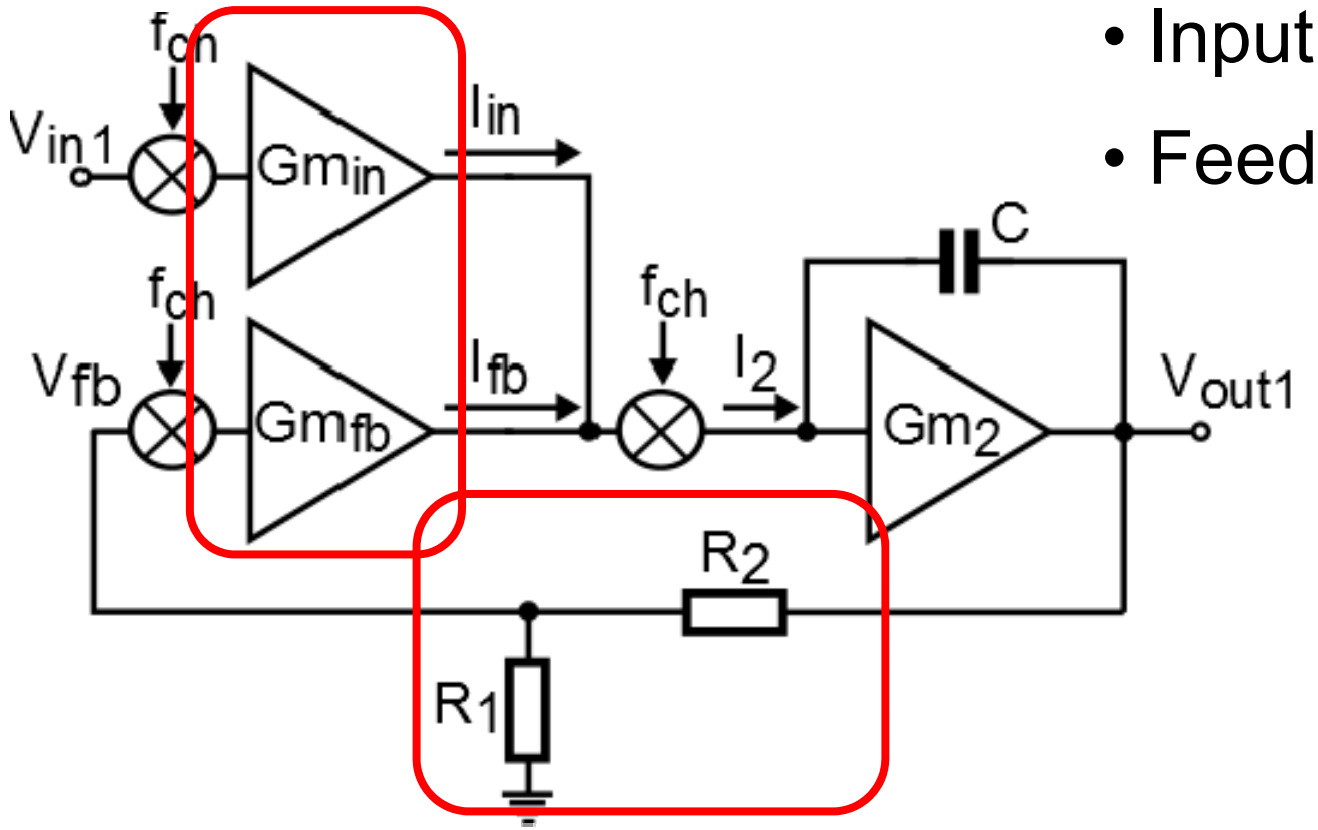
[van den Dool, '93]

Chopper modulation



- Chopper modulation added to remove offset and *1/f* noise

Gain mismatch sources

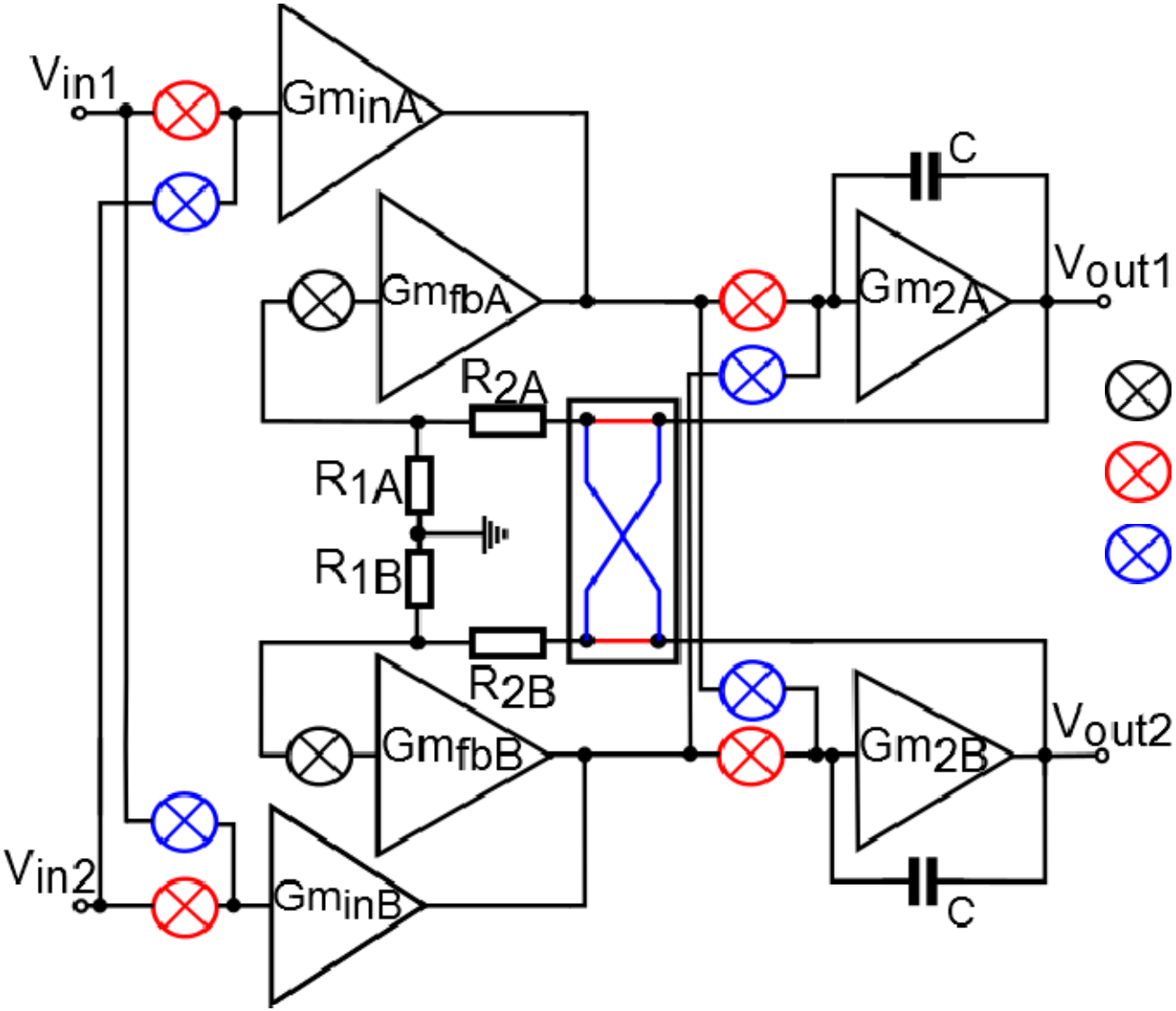


- Input Gm's
- Feedback network

- ΔGm/Gm = 0.15% requires ≈ 0.35 mm^2
- 2-channels interface
- Interested in ratio between outputs for angle measurement

Dynamic Element Matching

- Critical blocks swapped between channels

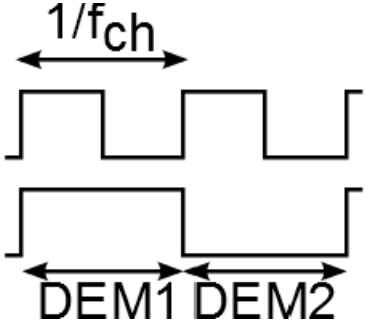


= always active

= active in DEM1

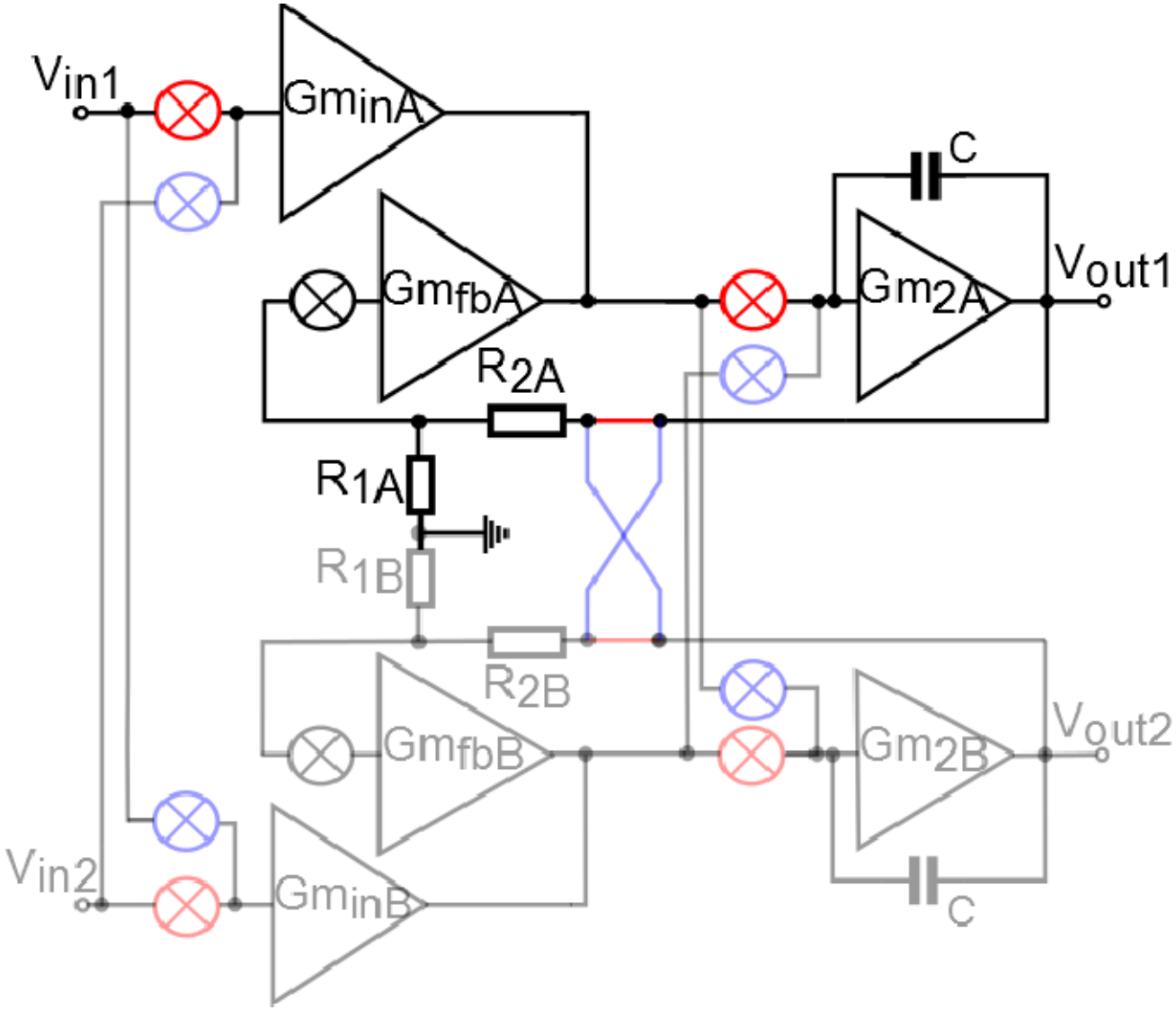
= active in DEM2

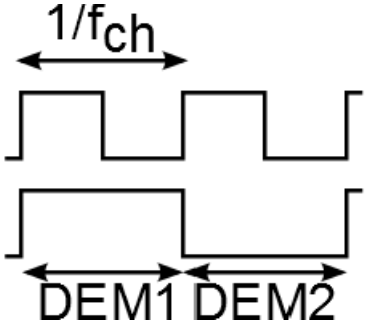
(otherwise Hi-Z)



Dynamic Element Matching

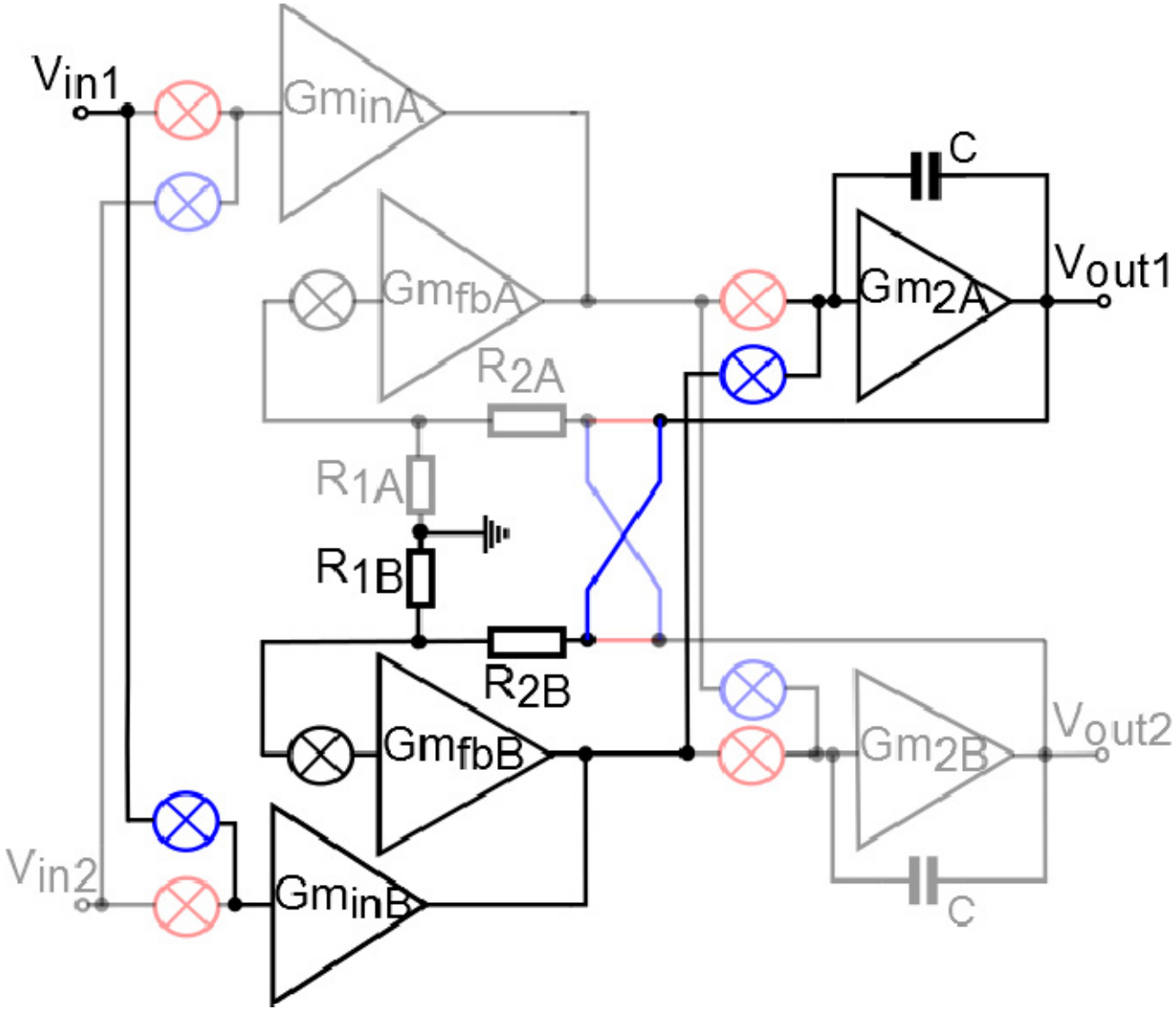
- V_{in1}: DEM1 phase

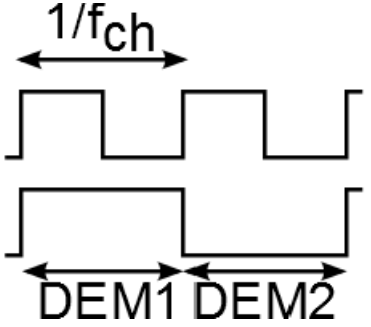




Dynamic Element Matching

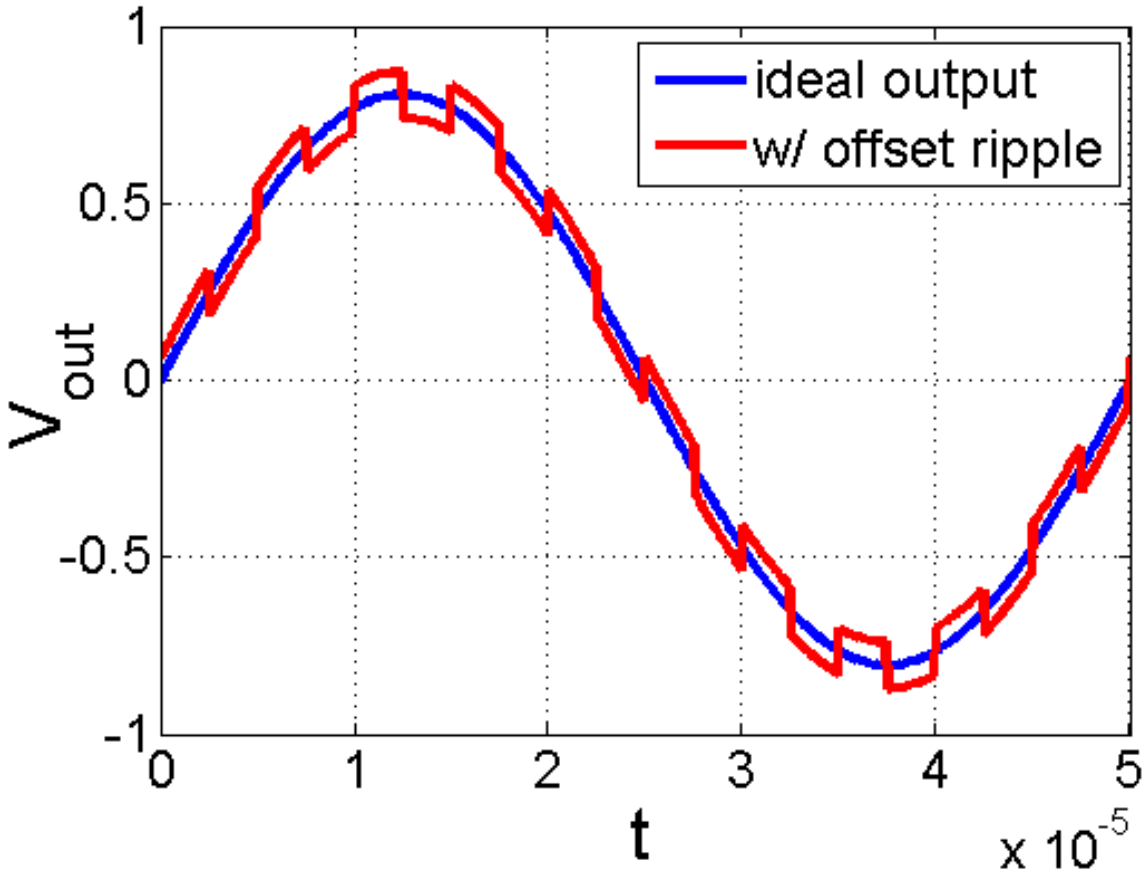
- V_{in1}: DEM2 phase





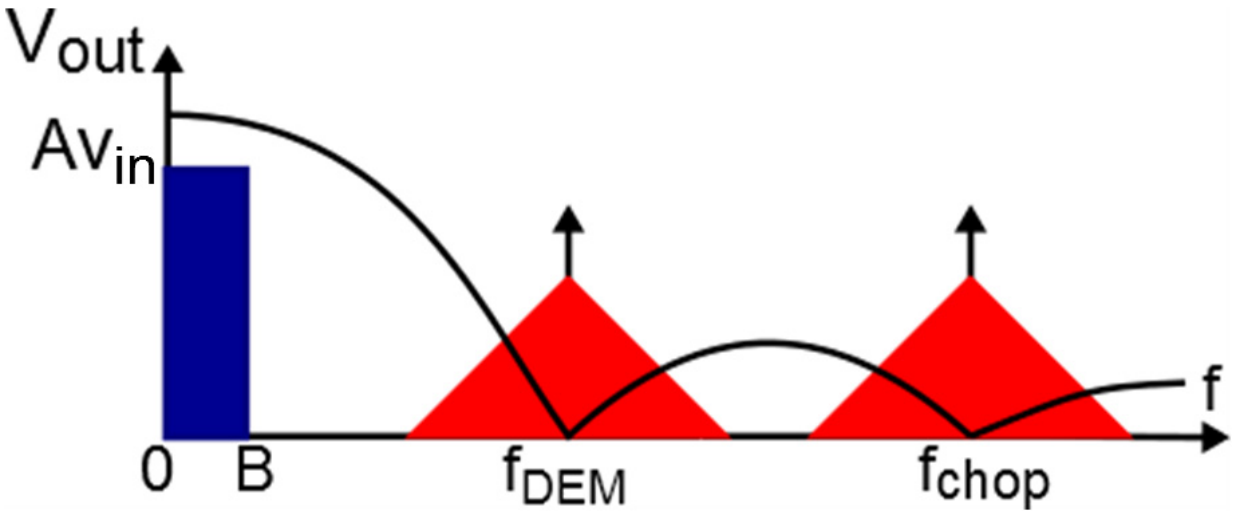
Ripple filtering

- **Usually removed**
  - E.g. ripple-reduction loop: area expensive
- **In this application:**
  - $V_{in,max}$ = 62 $mV_{pk,diff}$
  - $V_{out,max}$ = 0.9 $V_{pk,diff}$
  - Gain = 13
  - Ripple headroom = 96 mV
- **With this choice:**
  - DR loss is ≈ 1 dB

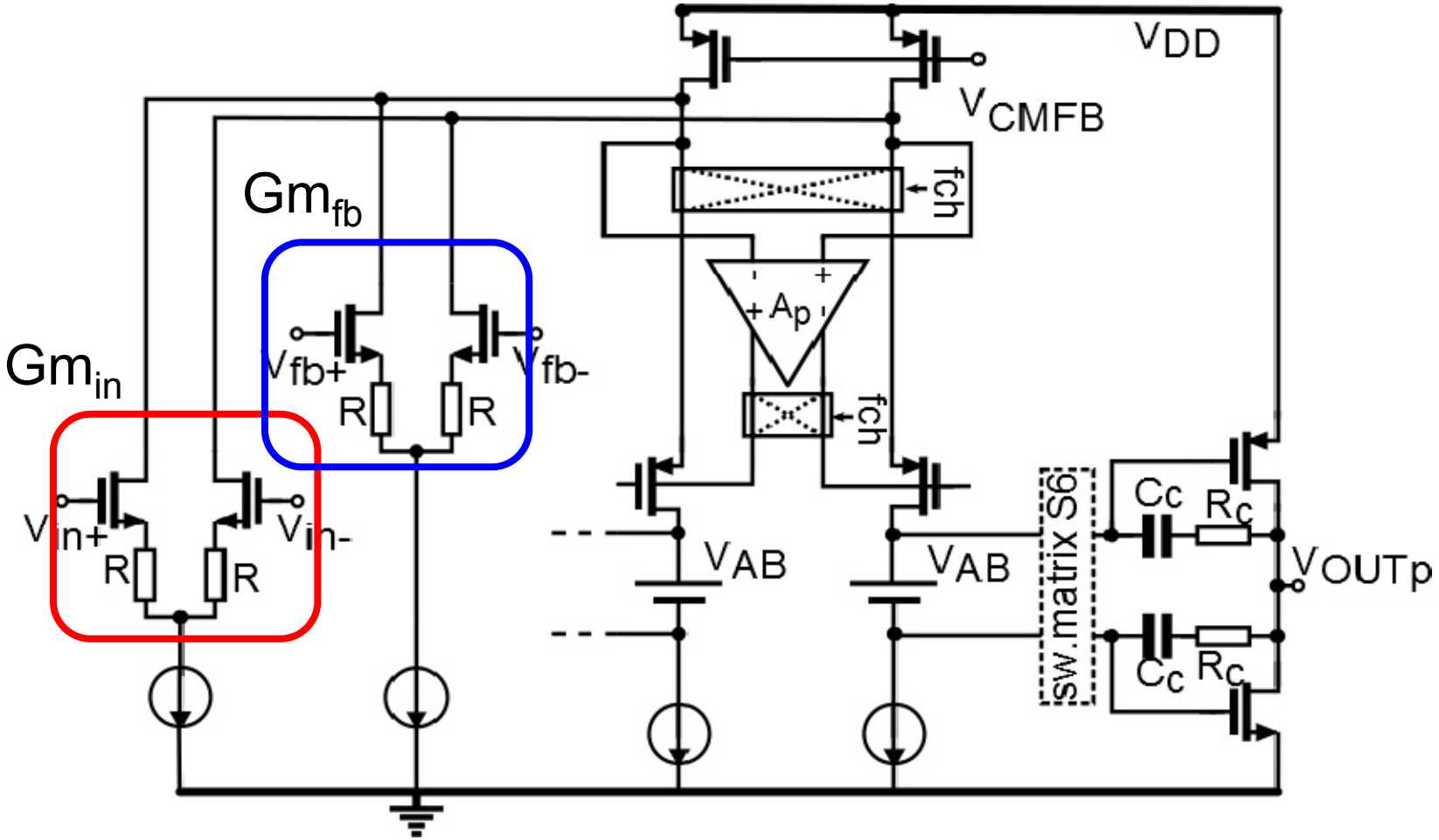


Ripple filtering

- **Filtering can be operated in the digital domain**
  - To relax filter specs: DEM frequency >> signal BW (20 kHz)
  - DEM frequency = 100 kHz
  - E.g. *sinc* filtering (max in-band loss is 0.6 dB)

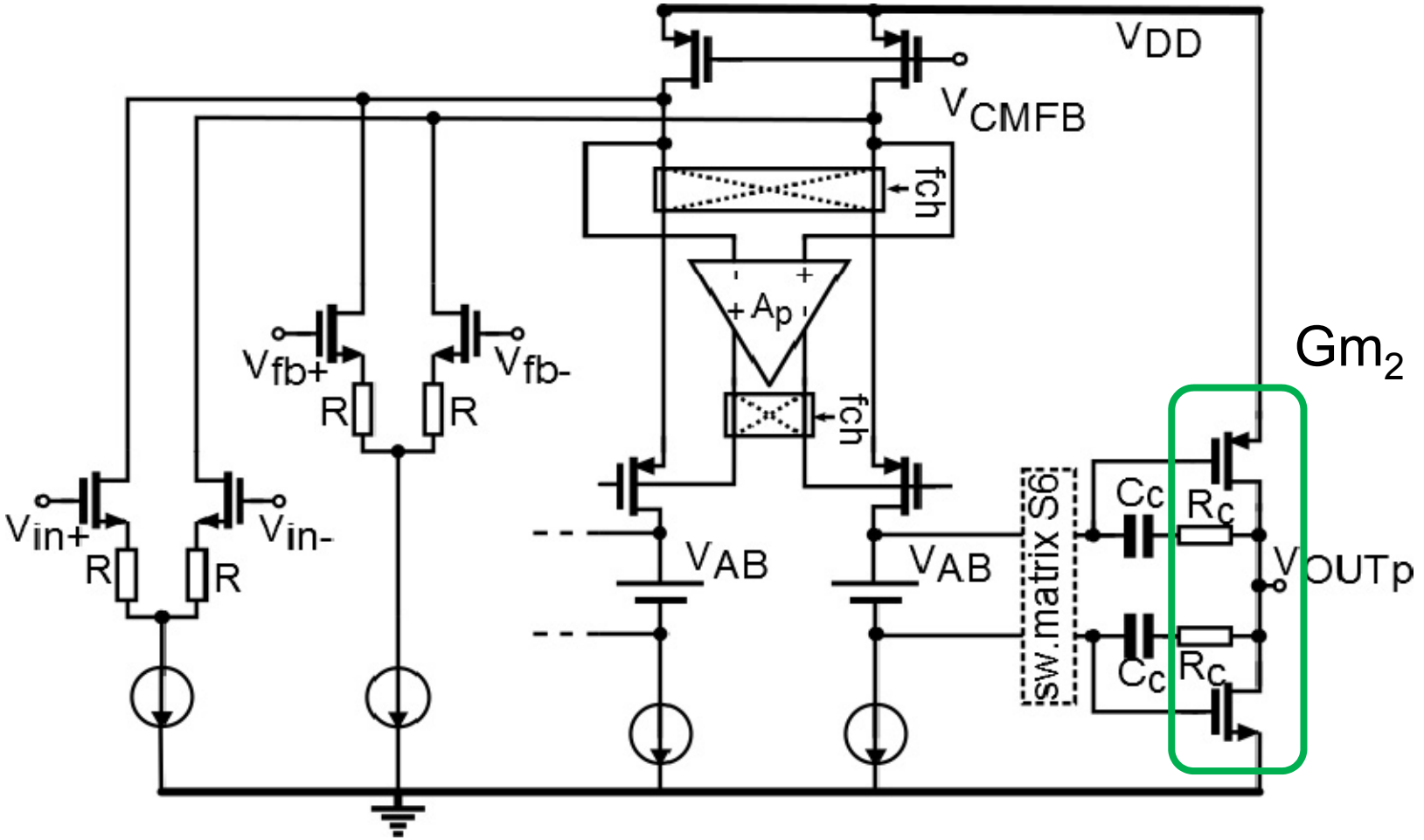


Schematic design



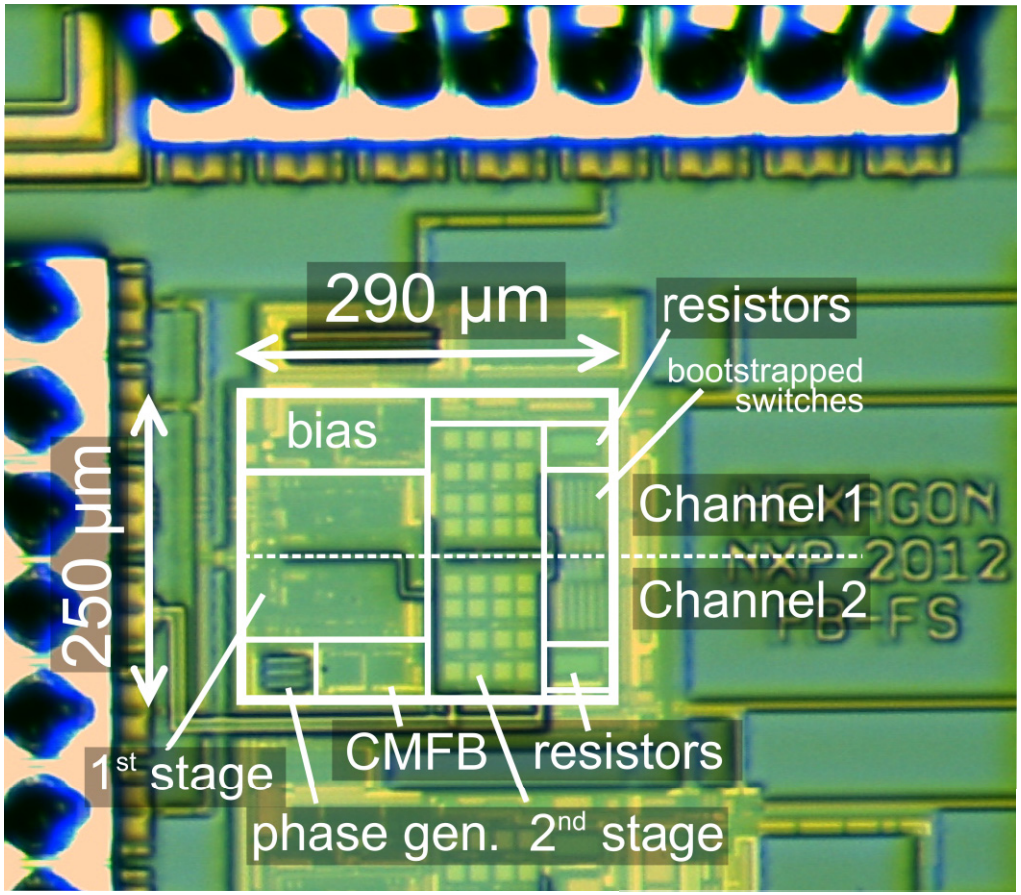
- Source degeneration to increase input linear range
- Gain boosted folded cascode [Kashmiri, '09]

Schematic design



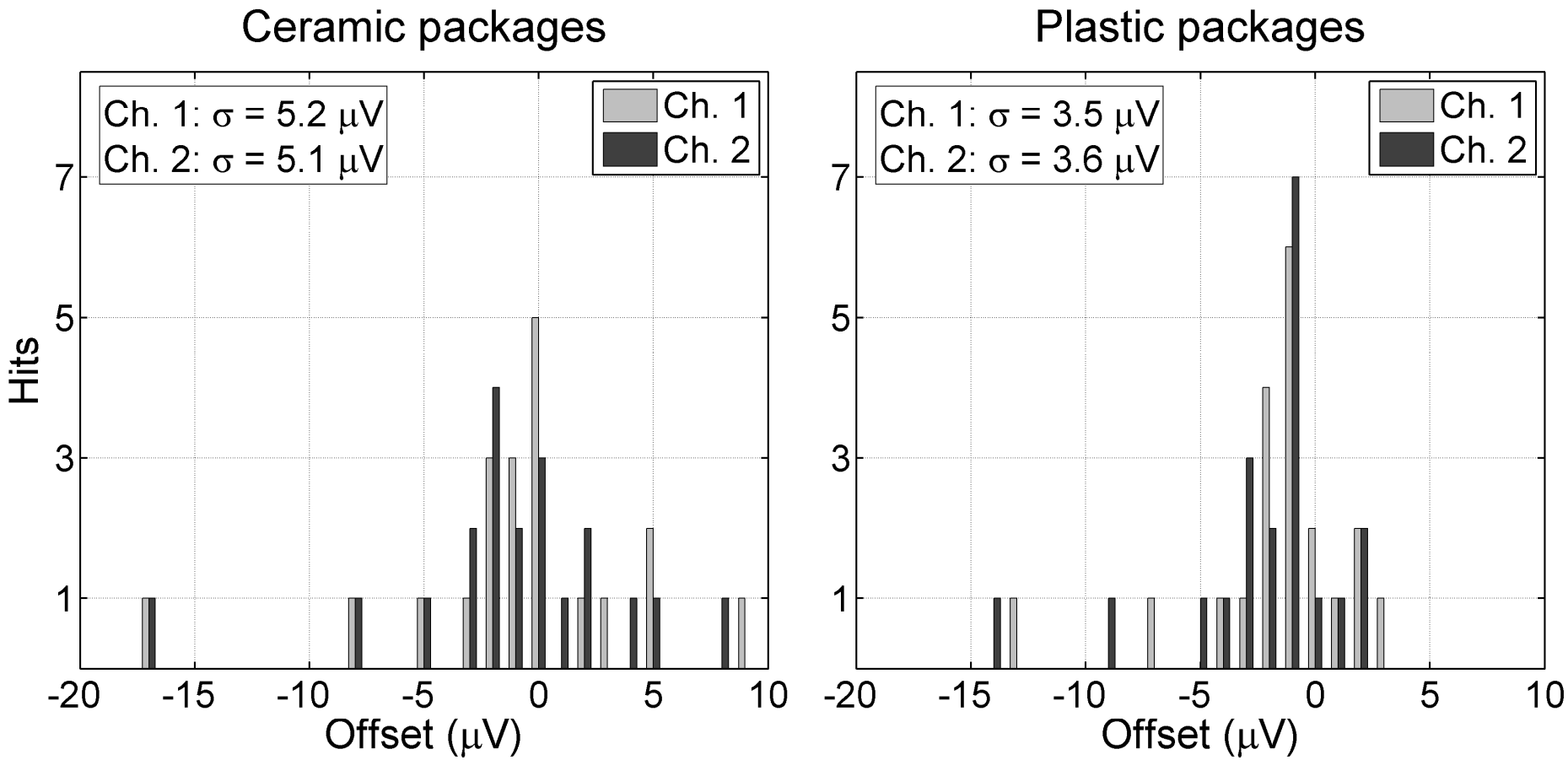
- Class AB output stage (G_{m2}) biased by floating battery V_{AB}

0.16 µm CMOS realization



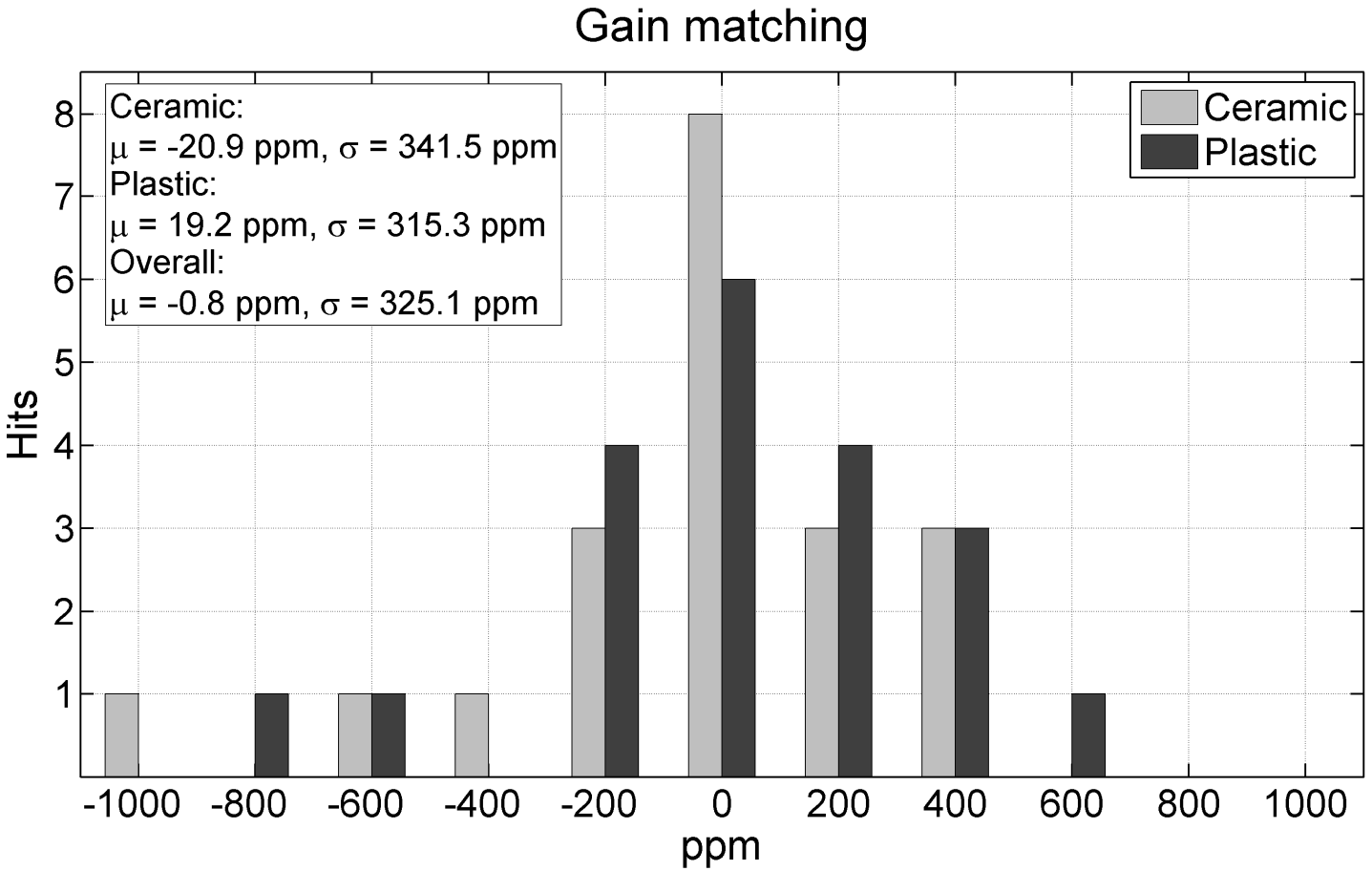
- SSMC 0.16 µm CMOS
- 1.8 V supply
- 320 µA each channel
- 0.07 mm^2 active area
- 40 Samples tested
  - 20 ceramic DIL package
  - 20 plastic DIL package

Results: offset



- Input offset lower than 17 μV
- Plastic and ceramic package show similar offset

Results: gain matching



- Gain matching measured at an input frequency of **20 kHz**
- Gain matching is better than 0.1% (1000 ppm)

Performance summary

Offset	**< 17 µV**
Gain matching	**0.1%**
Input noise PSD	18.7 nV/√Hz
NEF	12.9
CMRR	> 99 dB (up to 50 kHz)
PSRR	> 102 dB (up to 50 kHz)
Linearity (V_{in}=120 $mV_{pkpk,diff}$)	THD=-60dB @ f_{in}=21kHz
Crosstalk	-73 dB

Benchmark

	Akita ISSCC'13	Michel ISSCC'12	Wu JSSC'11	This work
Technology	0.18 µm	0.13 µm	0.7 µm	0.16 µm
Supply	1.5 V	1.2 V	5 V	1.8 V
f_{chop}	500 kHz	25 kHz	32 kHz	200 kHz
f_{DEM}	-	0.025 kHz	8 kHz	100 kHz
Offset	< 3.5 µV	< 5 µV	< 3 µV	< 17 µV
Gain matching	**-**	**±0.7%***	**0.08%***	**0.1%**
NEF	7.2	7.5	11.2	12.9
Die Area	**0.06 mm²**	**0.465 mm²**	**5 mm²**	**0.07 mm² (2 ch.)**

* extrapolated as gain error multiplied by √2

Conclusions

- **State-of-art performance**
  - Low noise: < 19 nV/√Hz
  - Power efficiency: NEF = 12.9
  - Low offset: < 17 μV
- **Dynamic matching of critical blocks enables:**
  - Channel gain matching better than 0.1%
  - Smallest state-of-art design (0.07 mm^2, 2 channels)

17.6: Envelope Modulator for Multimode Transmitters with AC-Coupled Multilevel Regulators

Patrik Arnò[1], Matthieu Thomas[2,3], Vladimír Molata[2,3], Tomáš Jeřábek[2]

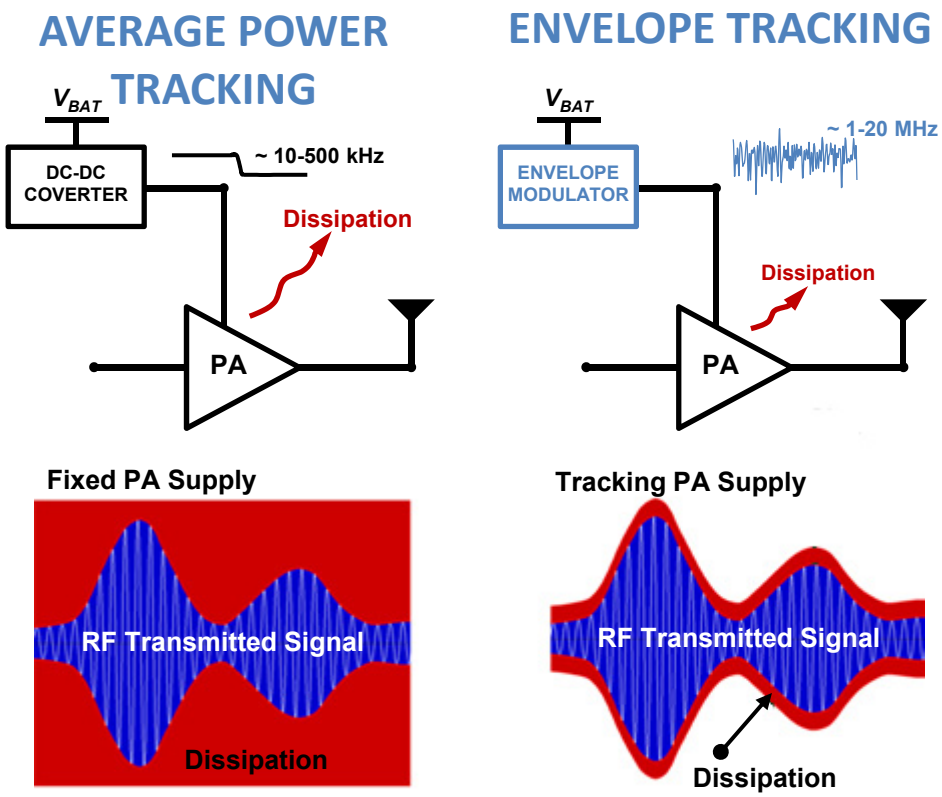
[1]STMicroelectronics, Grenoble, France,

[2]STMicroelectronics, Prague, Czech Republic,

[3]Czech Technical University, Prague, Czech Republic

Envelope Tracking Operation

Envelope Tracking is a power management technique for the improvement of RF PAs efficiency. It replaces the **static (or slowly varying) voltage supply** of RF PA with a **dynamic supply voltage**, which closely tracks the "envelope" of the RF signal



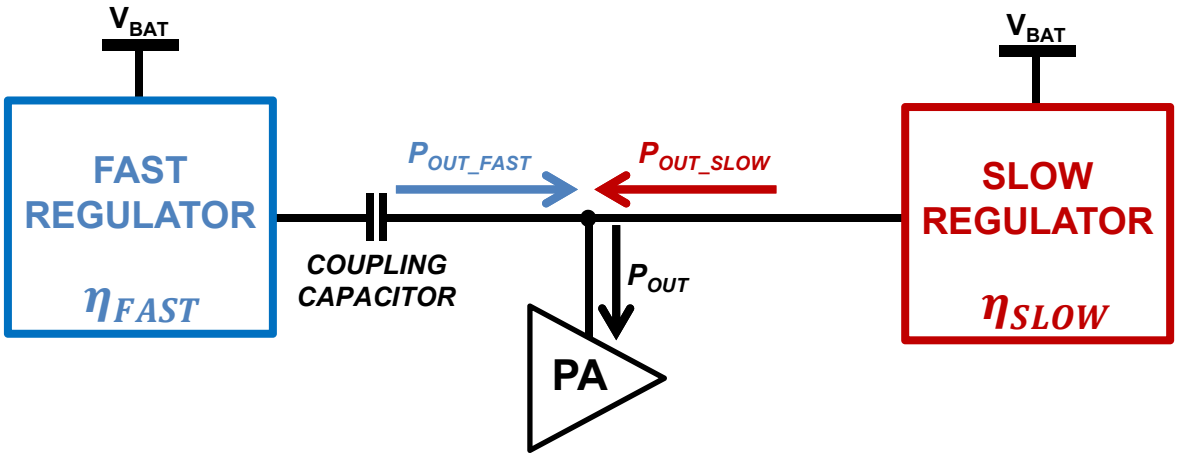
ENVELOPE MODULATOR characteristics:

- **High Efficiency: >80%**
- **Large Bandwidth: up to 20MHz**
- **Low Noise**

Outline

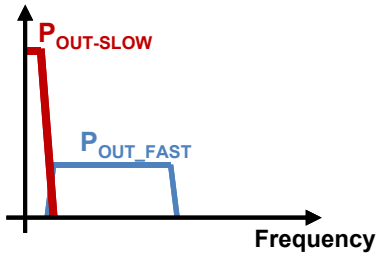
- Parallel AC-coupled regulators: Efficiency
- Parallel AC-coupled regulators: Regulation loops
- Detailed description of proposed ET modulator
- Physical Implementation
- Measurement Results
- Conclusions

Parallel AC-coupled regulators: Efficiency



P_{OUT_SLOW}: HIGH POWER, LOW FREQUENCY

P_{OUT_FAST}: LOW POWER, HIGH FREQUENCY



$$k = \frac{P_{OUT\_FAST}}{P_{OUT\_SLOW}} \ll 1$$

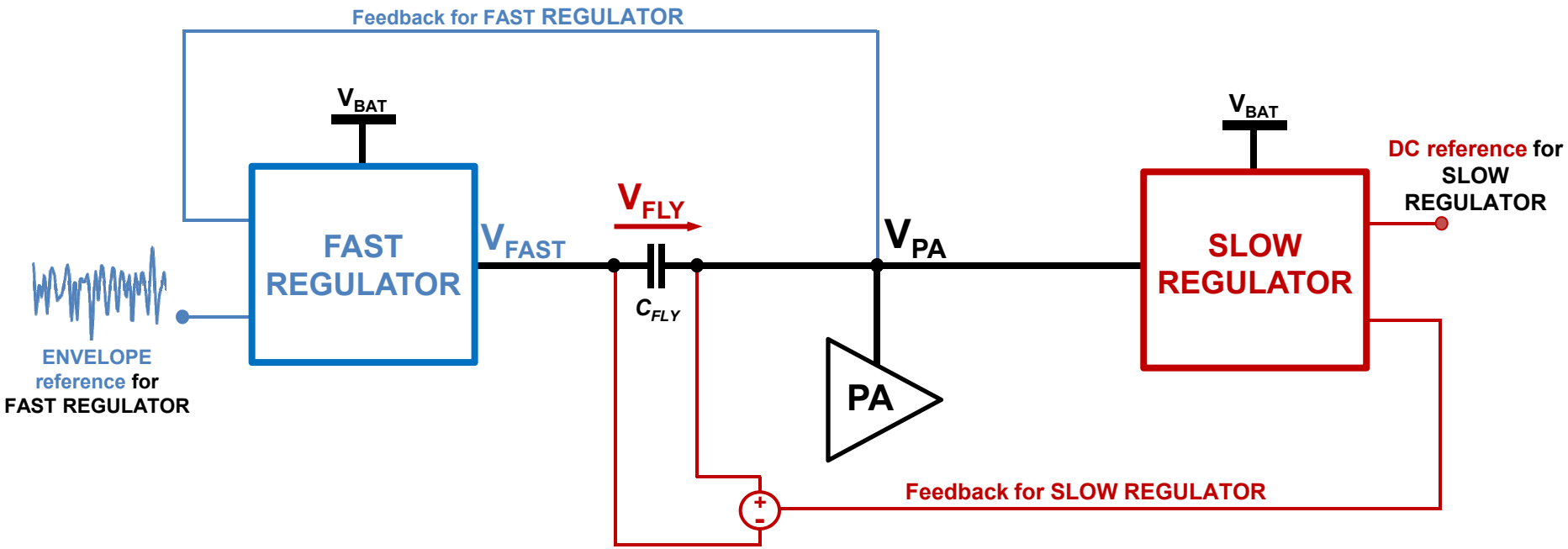
For LTE10 k < 15%

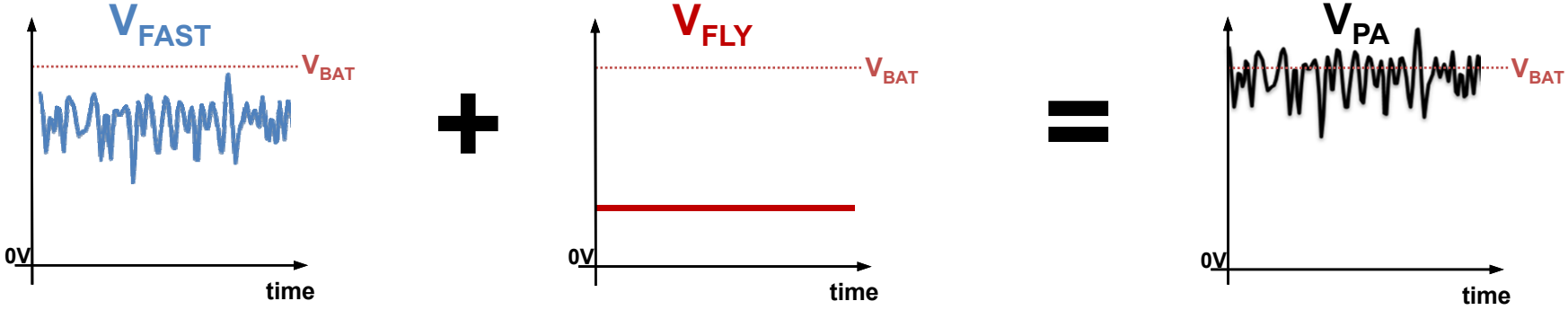
TOTAL EFFICIENCY

$$\frac{1}{\eta_{TOT}} = \frac{k}{k+1} \cdot \frac{1}{\eta_{FAST}} + \frac{1}{k+1} \cdot \frac{1}{\eta_{SLOW}}$$

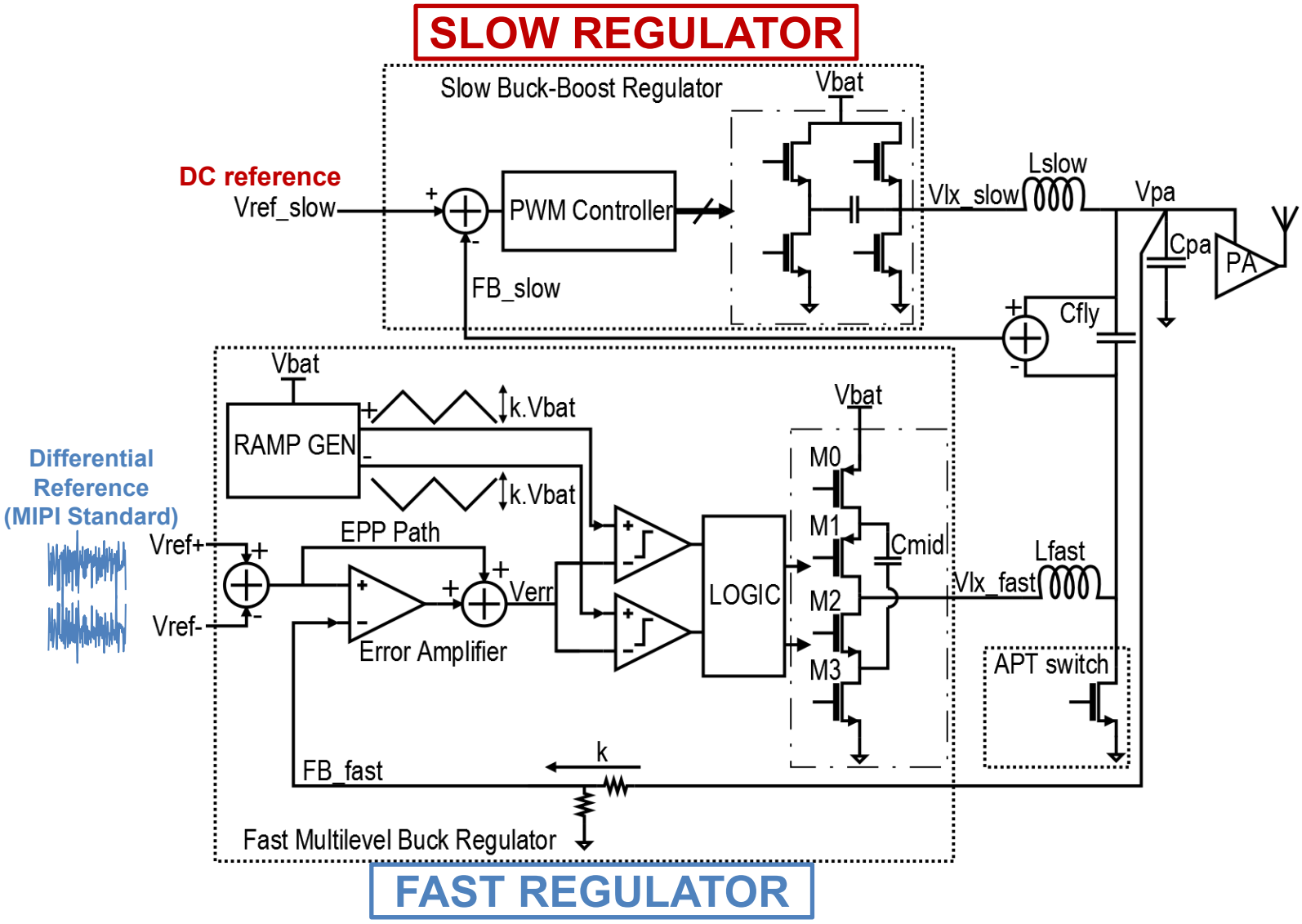
SLOW contribution is dominant

Parallel AC-coupled regulators: Loops

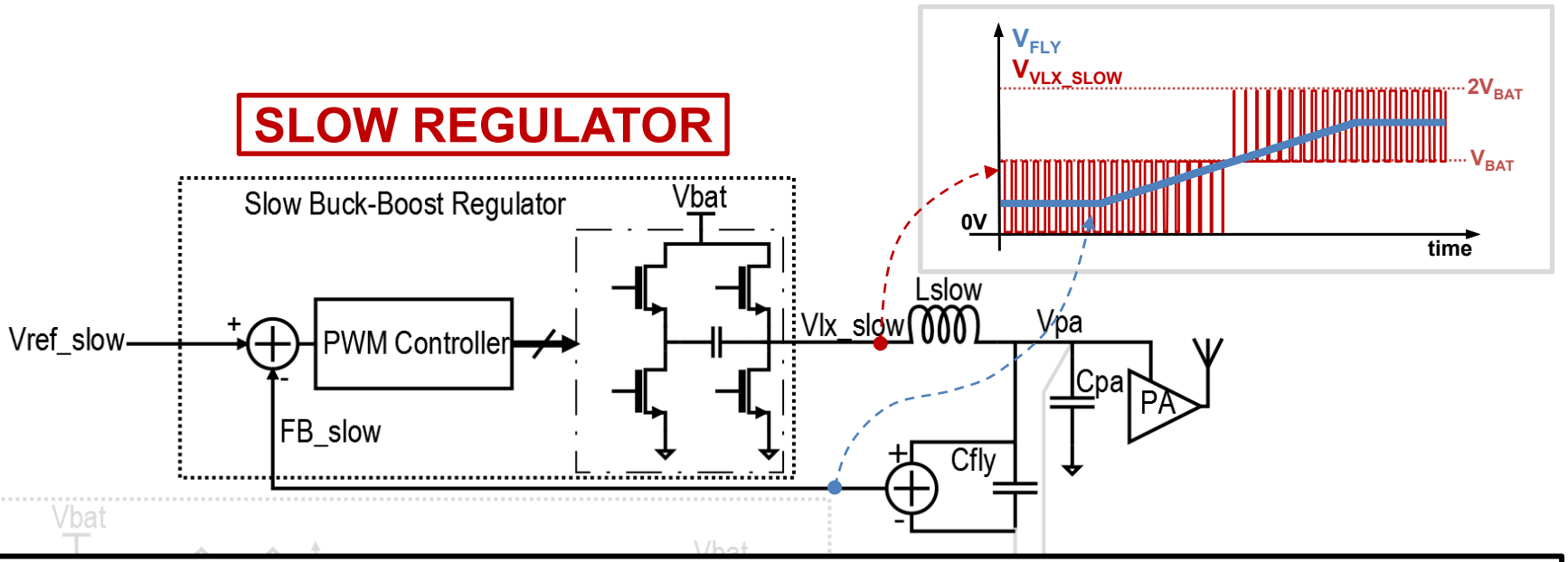




ET Modulator Diagram



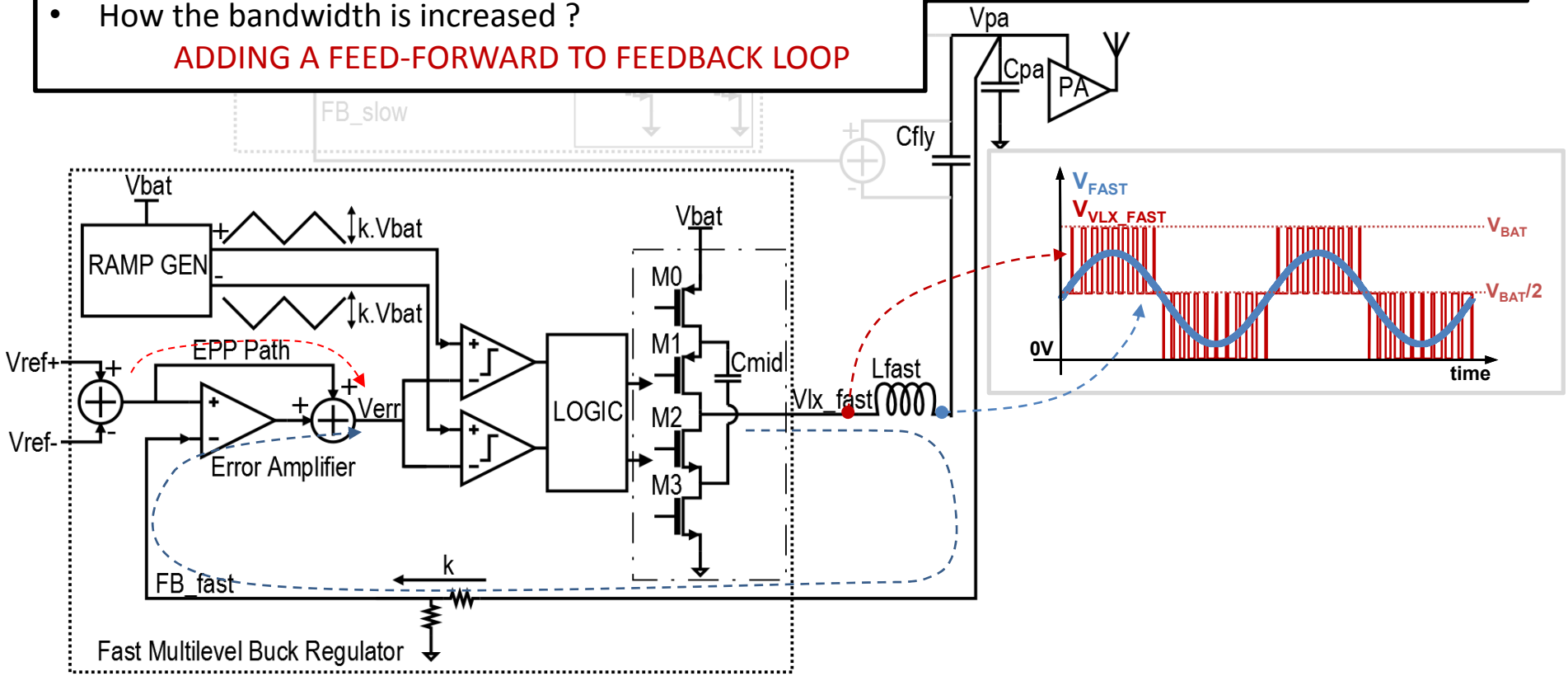
SLOW Low Ripple Buck-Boost Regulator



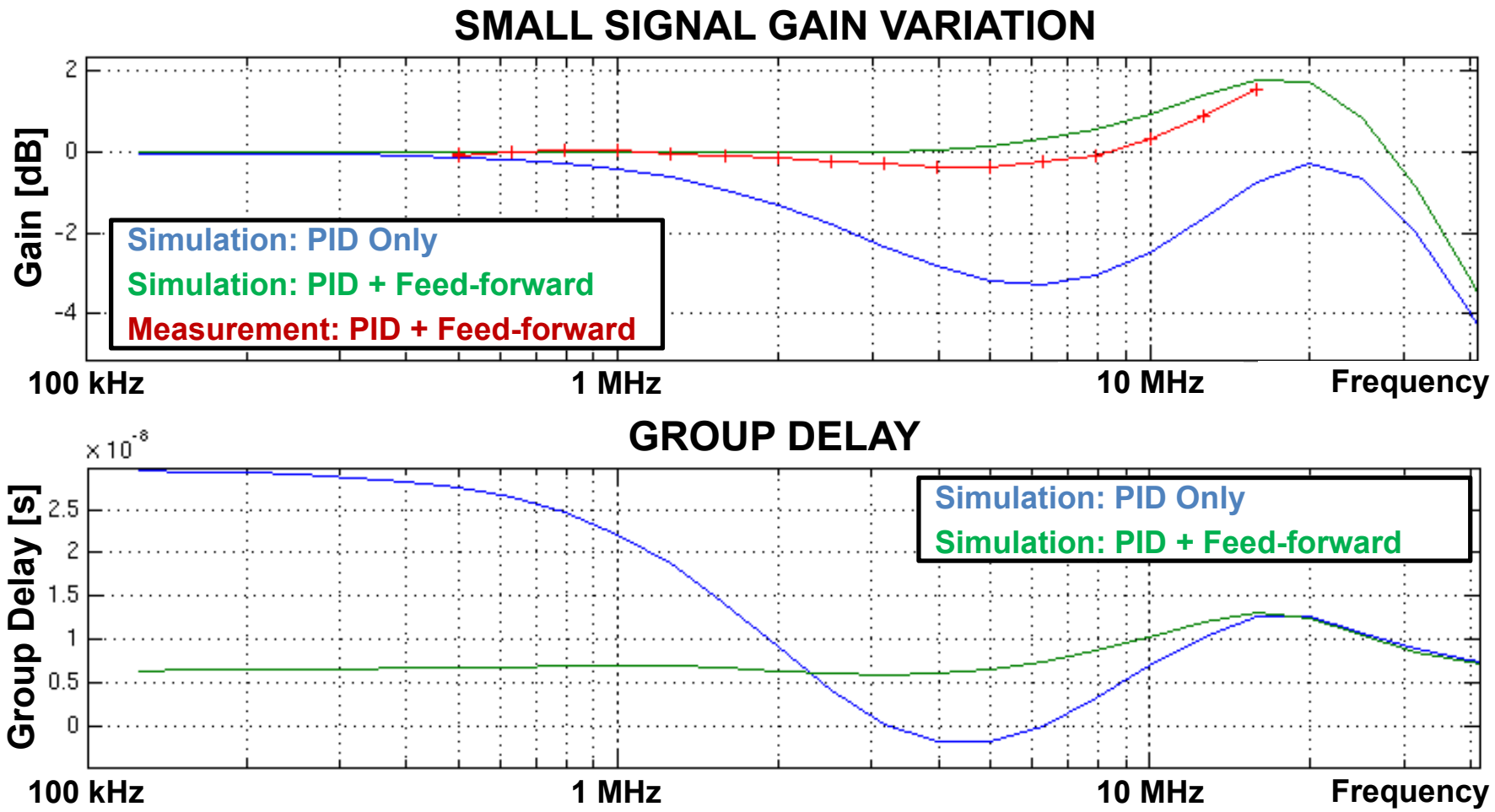
- Why a Buck-Boost regulator instead of a simple Buck ?
  - FOR VERY LOW CUTOFF BATTERIES
  - FOR GSM PAs IN MULTIMODE TRANSMITTERS. MAX. OUTPUT CURRENT 2A DC
- How multilevel operation works ?
  - POWER STAGE SWITCHES ON 3 LEVELS: GROUND, V_{BAT} and $2 \cdot V_{BAT}$
- How low ripple operation is achieved ?
  - THIS STRUCTURE BEHAVES LIKE A STANDARD BUCK REGULATOR. THE OUTPUT IS ALWAYS CONNECTED TO THE COIL AND THE OUTPUT CURRENT IS CONTINOUS

FAST 3-levels Buck Regulator

- Why a switching regulator instead of linear amplifier?
  TO IMPROVE POWER EFFICIENCY
- Why multilevel ?
  TO REDUCE OUTPUT RIPPLE. RIPPLE DIVIDED BY: (num. of levels -1)
- How multilevel operation works ?
  POWER STAGE SWITCHES ON 3 LEVELS: GROUND, $V_{BAT}/2$ and V_{BAT}
- How the bandwidth is increased ?
  ADDING A FEED-FORWARD TO FEEDBACK LOOP



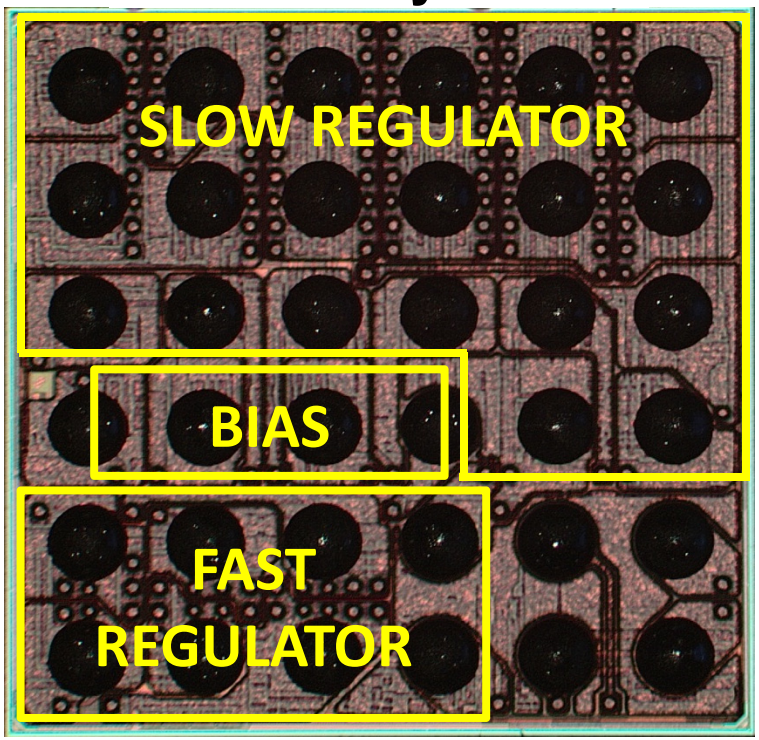
Modulator Transfer Function



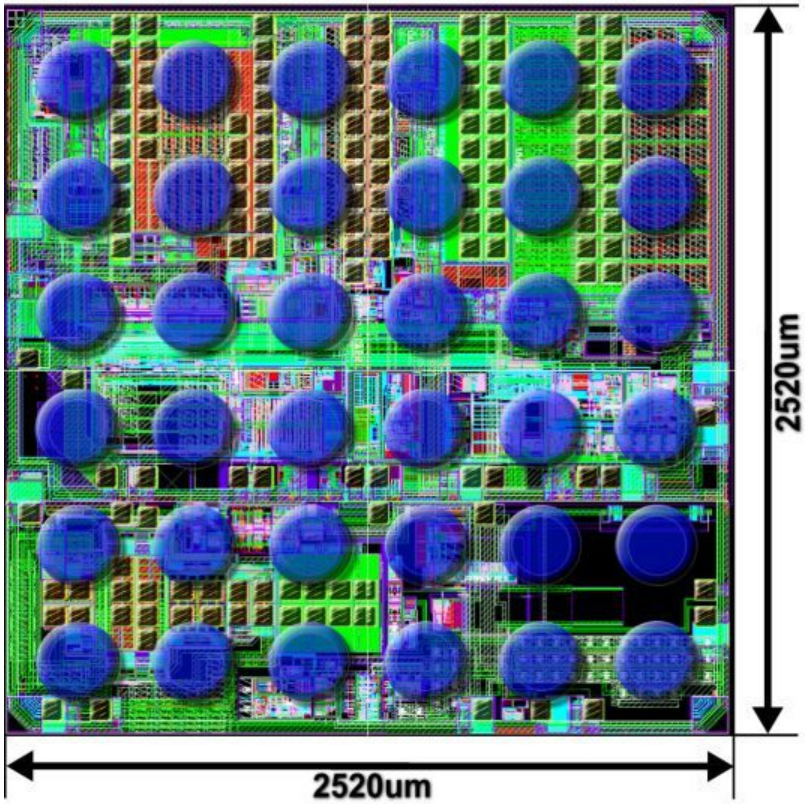
In the band 0.2-10MHz, the Feed-forward helps to reduce gain variation from 3.3dB to 1dB and group delay variation from 27ns to 3.8ns

Physical Implementation

X-Rays

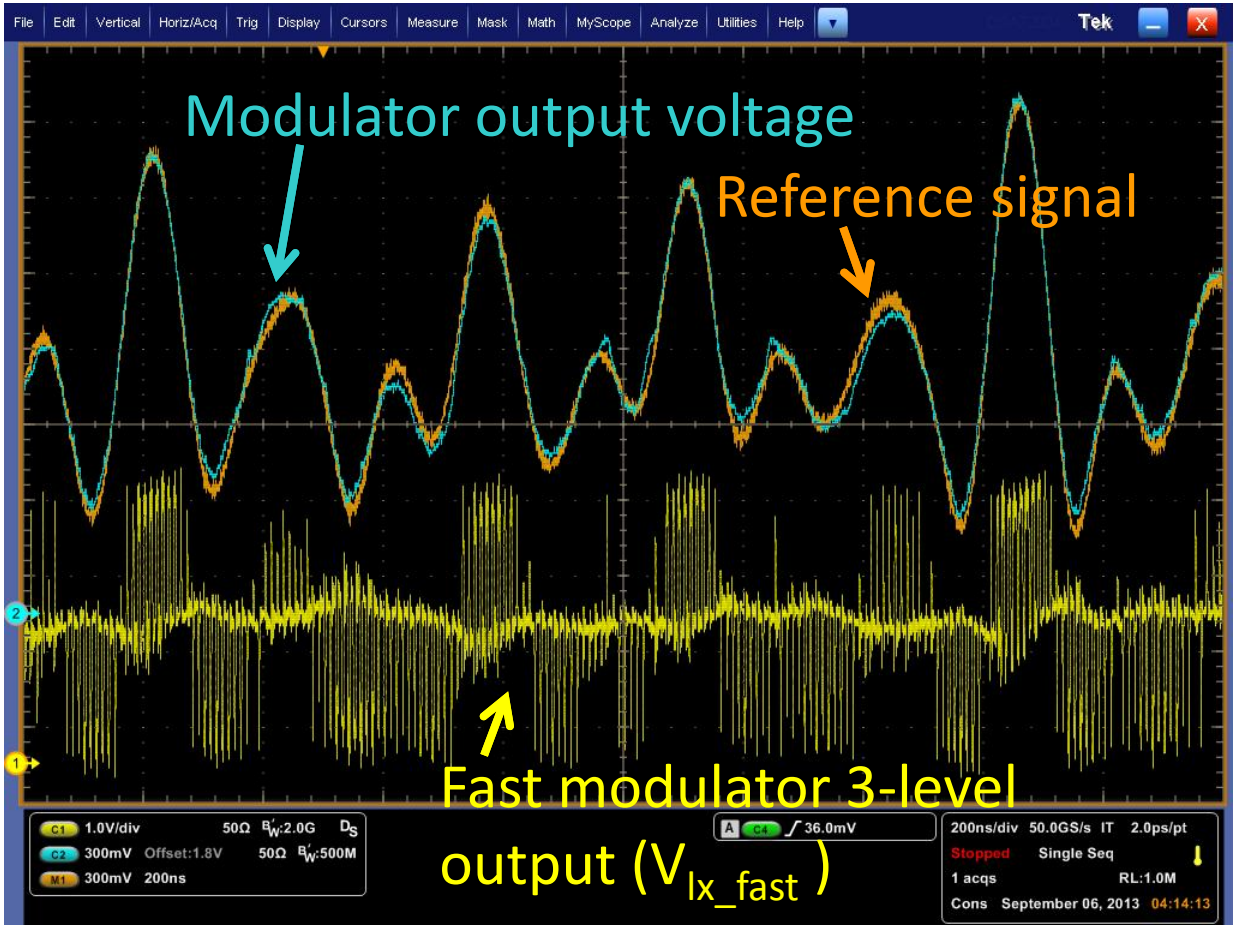


Layout Sketch



- Modulator implemented in 0.13µm, 4.8V, n-well CMOS technology from **STMicroelectronics (HCMOS9A)**
- The package is a 400µm pitch wafer level chip scale package (WLCSP)

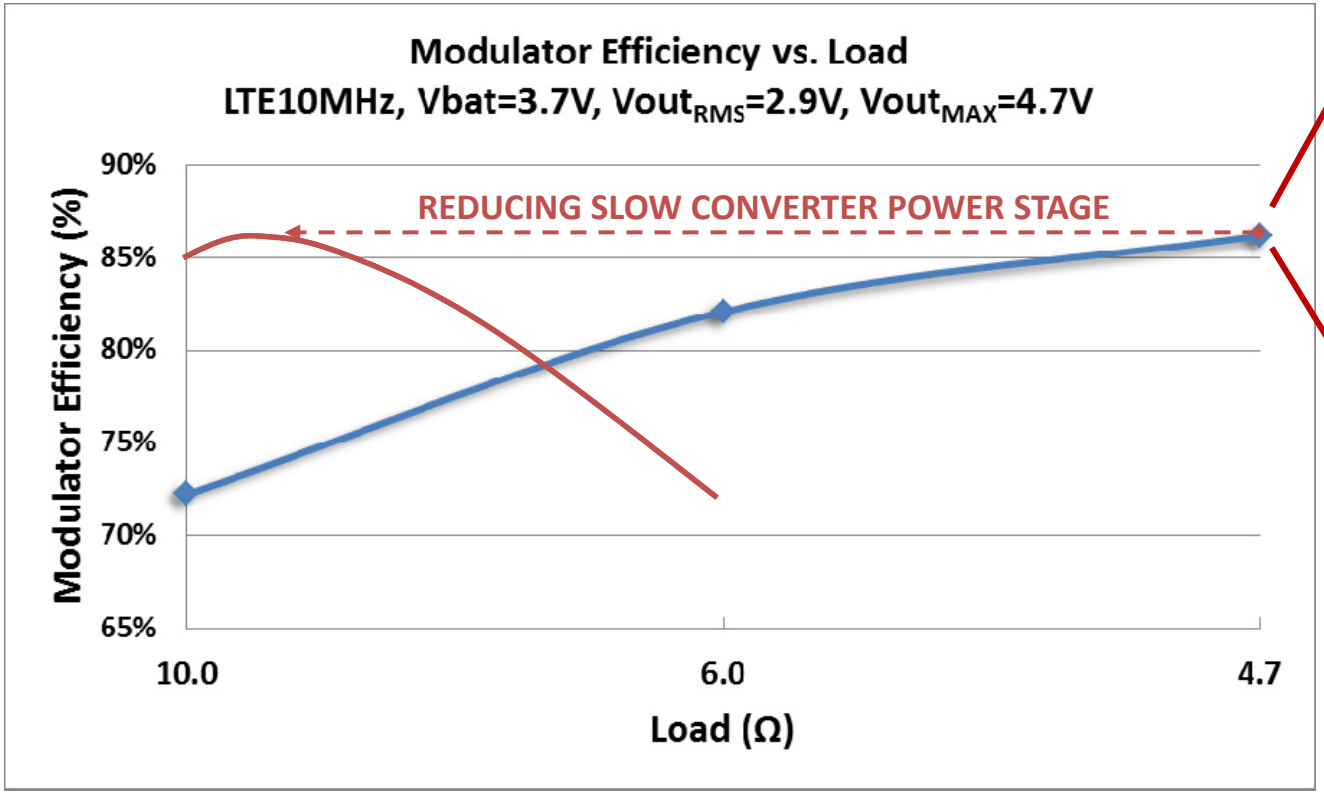
Measured Results



Tracking performance for LTE10 (6.7dB of PAPR) signal

FAST Regulator Switching Frequency 80 MHz

Modulator Efficiency vs. Load



Efficiency = 86.2%

V_{BAT}=3.7V

V_{OUT_MAX}=4.7V

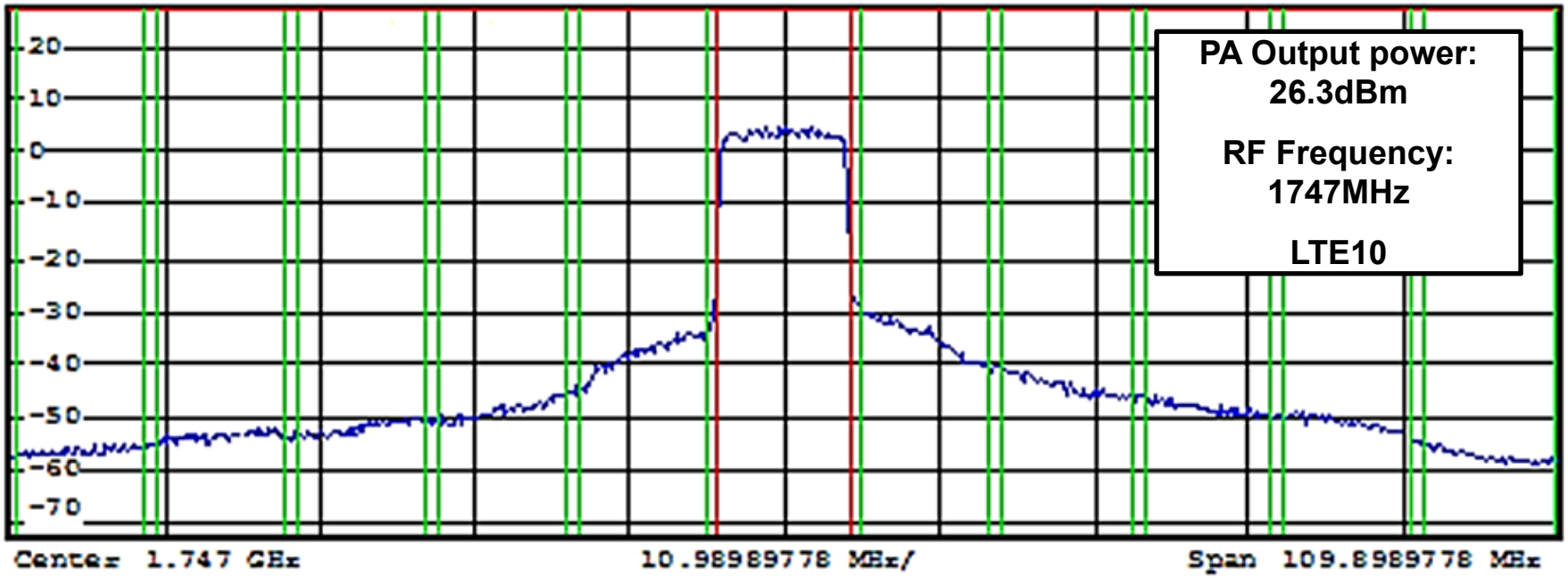
V_{OUT_RMS}=2.9V

I_{OUT_RMS}= 617mA

Efficiency for LTE10 (6.7dB of PAPR) signal

FAST Regulator Switching Frequency 80 MHz

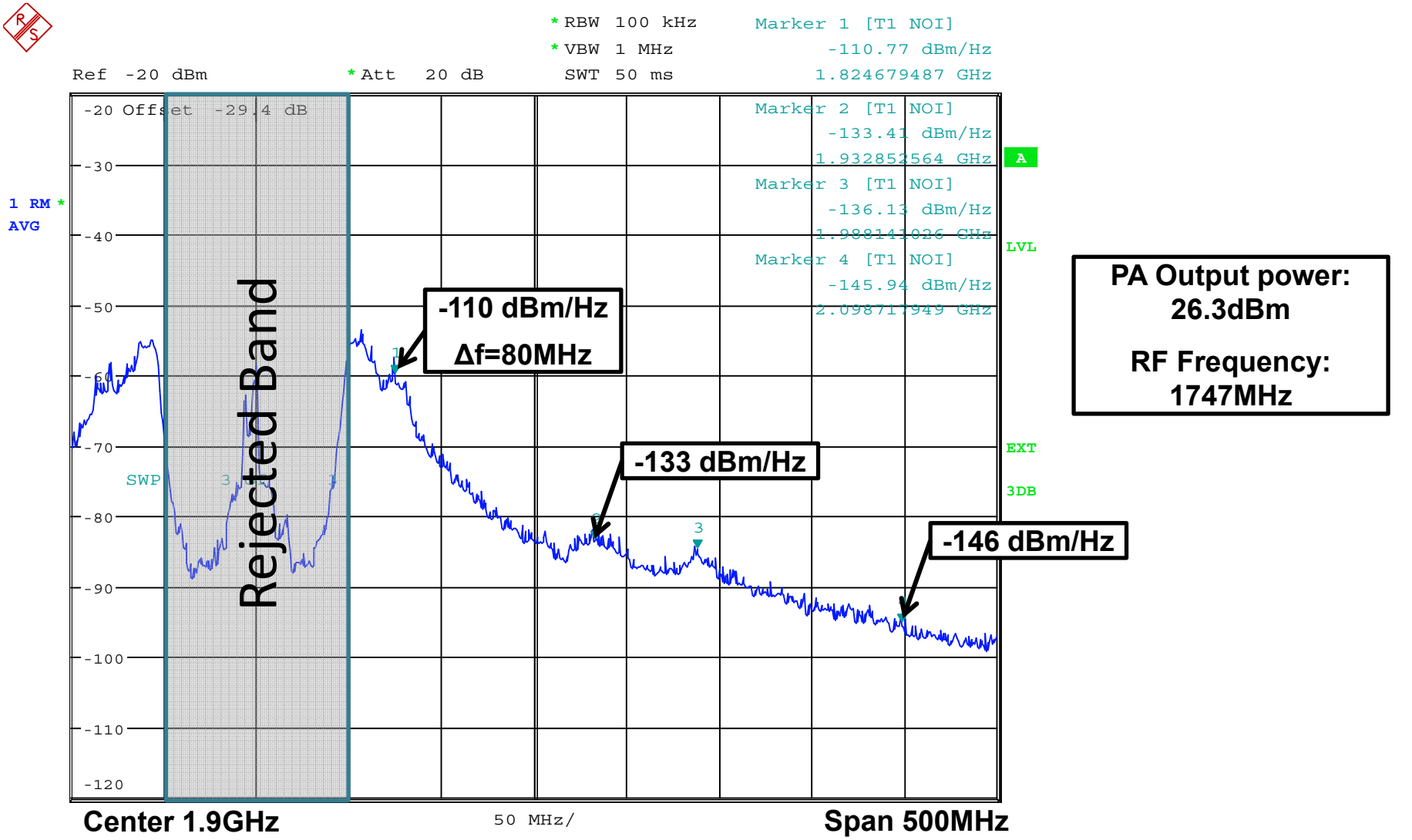
PA output spectrum



E-UTRA/LTE Square

Channel	Bandwidth	Spacing	Lower	Upper
Tx Channel	9.015 MHz		26.37 dBm	
Adjacent	9.015 MHz	10.000 MHz	-40.82 dB	-37.30 dB
Alternate	9.015 MHz	20.000 MHz	-52.17 dB	-47.28 dB
2nd Alt	9.015 MHz	30.000 MHz	-55.57 dB	-51.62 dB
3rd Alt	9.015 MHz	40.000 MHz	-57.20 dB	-54.45 dB
4th Alt	9.015 MHz	50.000 MHz	-60.04 dB	-60.74 dB

PA RF Output Noise



PA Output power: 26.3dBm

RF Frequency: 1747MHz

Comparison

Reference	Protocol	RF Output Power [dBm]	PAPR 0.01% [dB]	Technology [µm]	Modulator Efficiency [%]	Supply Voltage [V]	Combined Efficiency [%]	ACLR [dBc]
This work	LTE 10MHz	26.3	6.7	0.13	86.2 ##	3.8	39 **	-40
[2]	HSUPA R6 5MHz	26	6.7	0.15	80	3.8	37	-40
[5]	LTE 10MHz	29.7	6	0.15	82	4.5	N/A	N/A
[6]	LTE 10MHz	27	6.44	0.18	76.3	N/A	39.8	-35.7

Maximum efficiency achieved on resistive load (4.7Ohm])

** 2 stages PA. Fist stage directelly connected to 3.8V, second stage supplied by ET modulator

[2] P. Riehl, P. Fowers, H.-P. Hong and M. Ashburn, "An AC-coupled hybrid envelope modulator for HSUPA transmitters with 80% modulator efficiency," in ISSCC Digest of Technical Papers, 2013

[5] M. Hassan, L. Larson, V. Leung and P. Asbeck, "A Combined Series-Parallel Hybrid Envelope Amplifier for Envelope Tracking Mobile Terminal RF Power Amplifier Applications," Solid-State Circuits, IEEE J., vol. 47, no. 5, pp. 1185-1198, May 2012

[6] D. Kim, Y. Cho, D. Kang, B. Park and B. Kim, "Envelope-Tracking Two-Stage Power Amplifier With Dual-Mode Supply Modulator for LTE Applications," Microwave Theory Techniques, IEEE Trans., vol. 61, no. 1, pp. 543-552, Jan 2013

Conclusions

- ET modulator based on multilevel switching regulators has been demonstrated
- Addition of Feed-Forward path to FAST Feedback loop reduces gain and group delay variations
- High current low noise Buck-Boost converter has been demonstrated
- Efficiency can be improved optimizing the SLOW REGULATOR for lower output current
- Solution available for integration

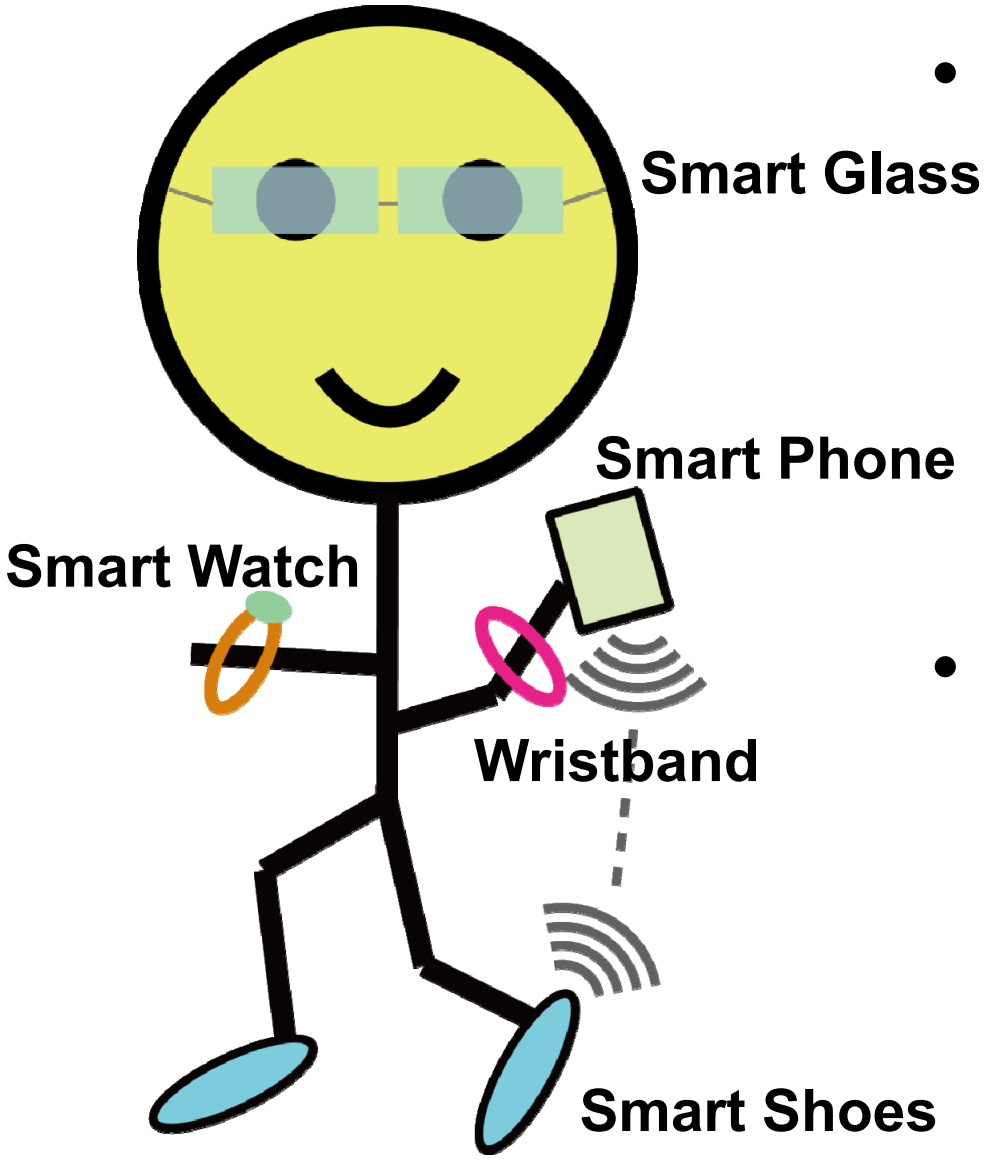
A 1.89nW/0.15V Self-charged XO for Real-time Clock Generation.

Keng-Jan Hsiao
MediaTek
Hsinchu, Taiwan

Outline

- Motivation
- System Architecture
- Circuit Details
- Experimental Results
- Conclusion

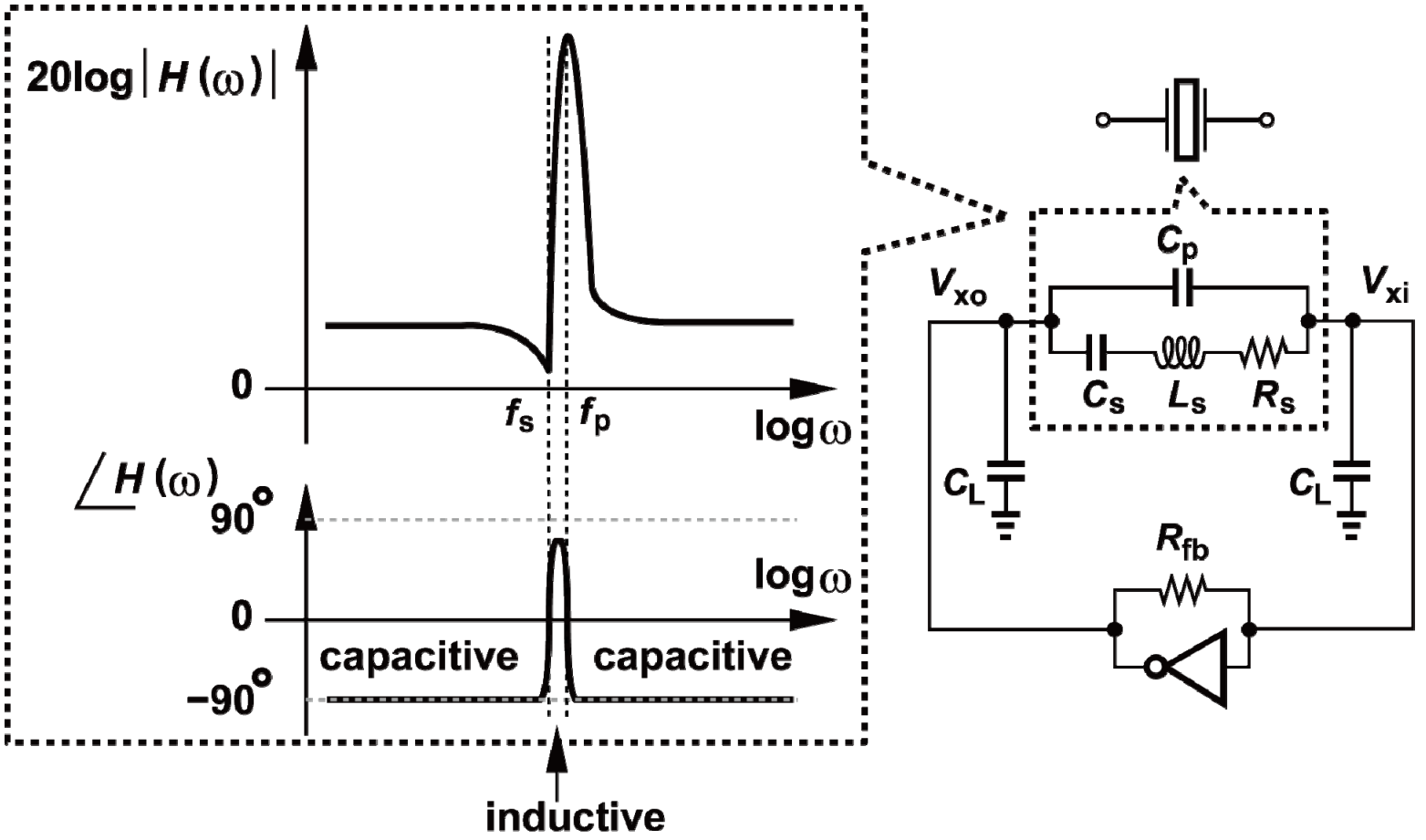
Verity Demands for the 32k Clock



- Main Function
  - Real-time clock
  - System standby clock

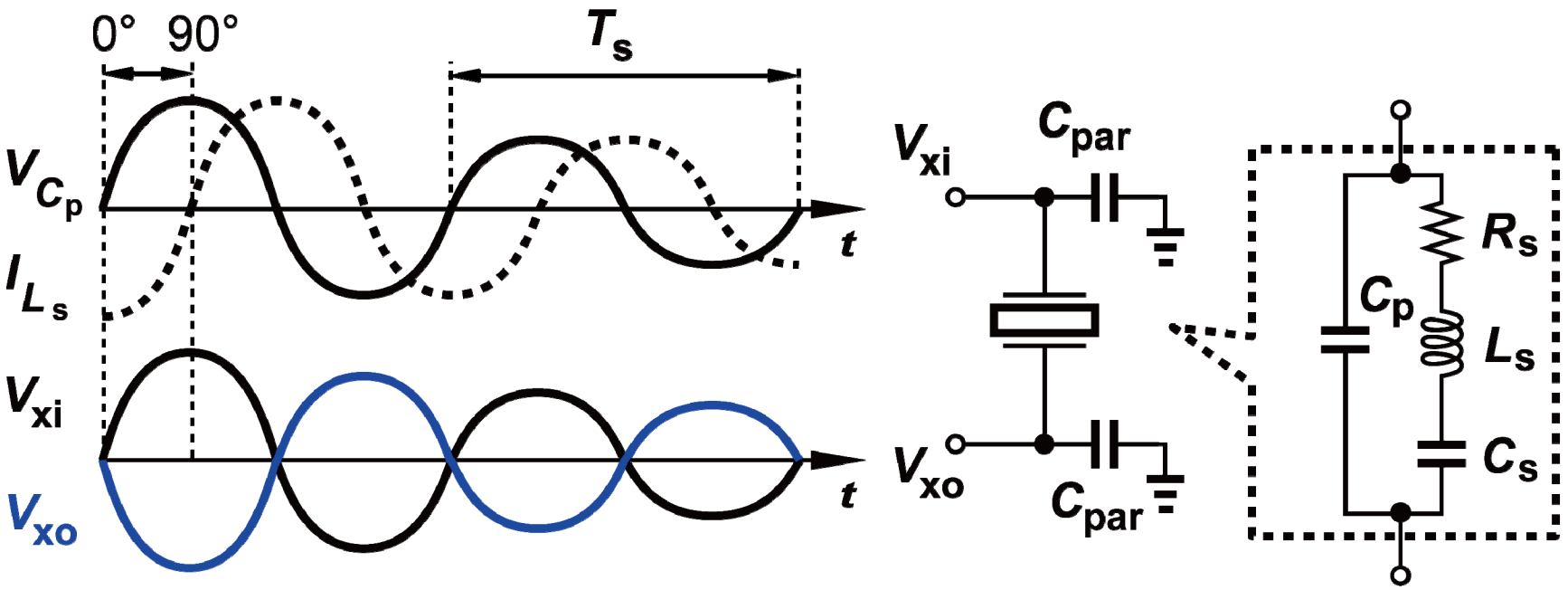
- Ultra-low power consumption for wearable devices.

XTAL & Pierce Oscillator



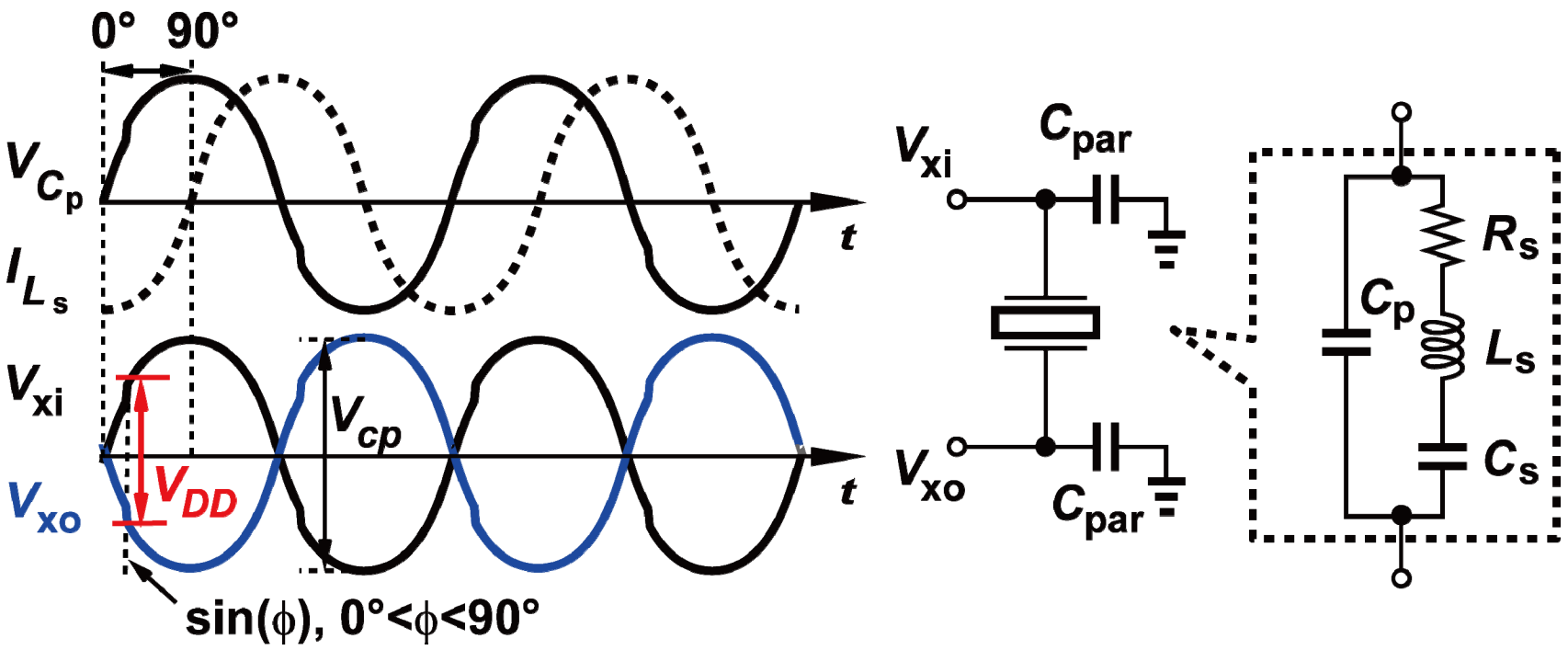
- R_{fb} and Inverting amp. consume power.

The Energy Flow Inside a XTAL



- **Energy transfers between the inductor and capacitors.**
- **The energy dissipated by R_s equals to $P_{R_s} \cdot T_s = 0.5 \cdot I_{L_s}{}^2 \cdot R_s \cdot T_s$.**

Recharge a XTAL

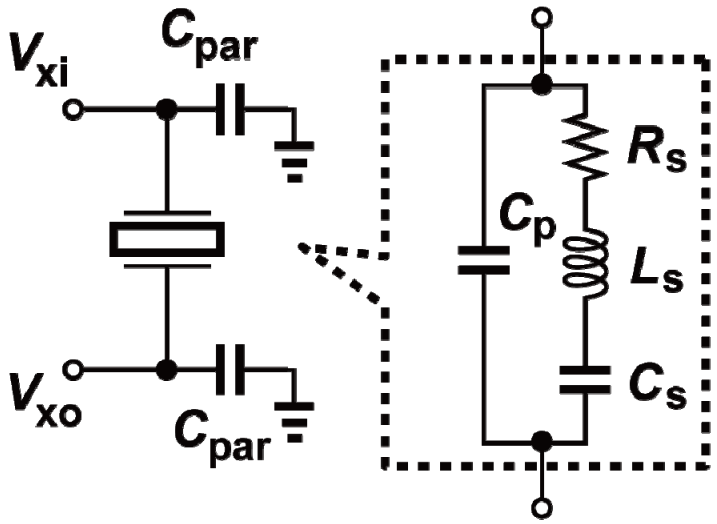


- **Energy charged to C_p & C_{par} = P_{R_s} x T_s.**

$$(V_{xo} - V_{xi}) = \frac{V_{DD}}{\left(\sin(\phi) + \sqrt{2\pi \cdot R_s \sqrt{\left(\frac{C_s + C_p + 0.5 \cdot C_{par}}{C_s}\right)\left(C_p + 0.5 \cdot C_{par}\right) / L_s}}\right)}$$

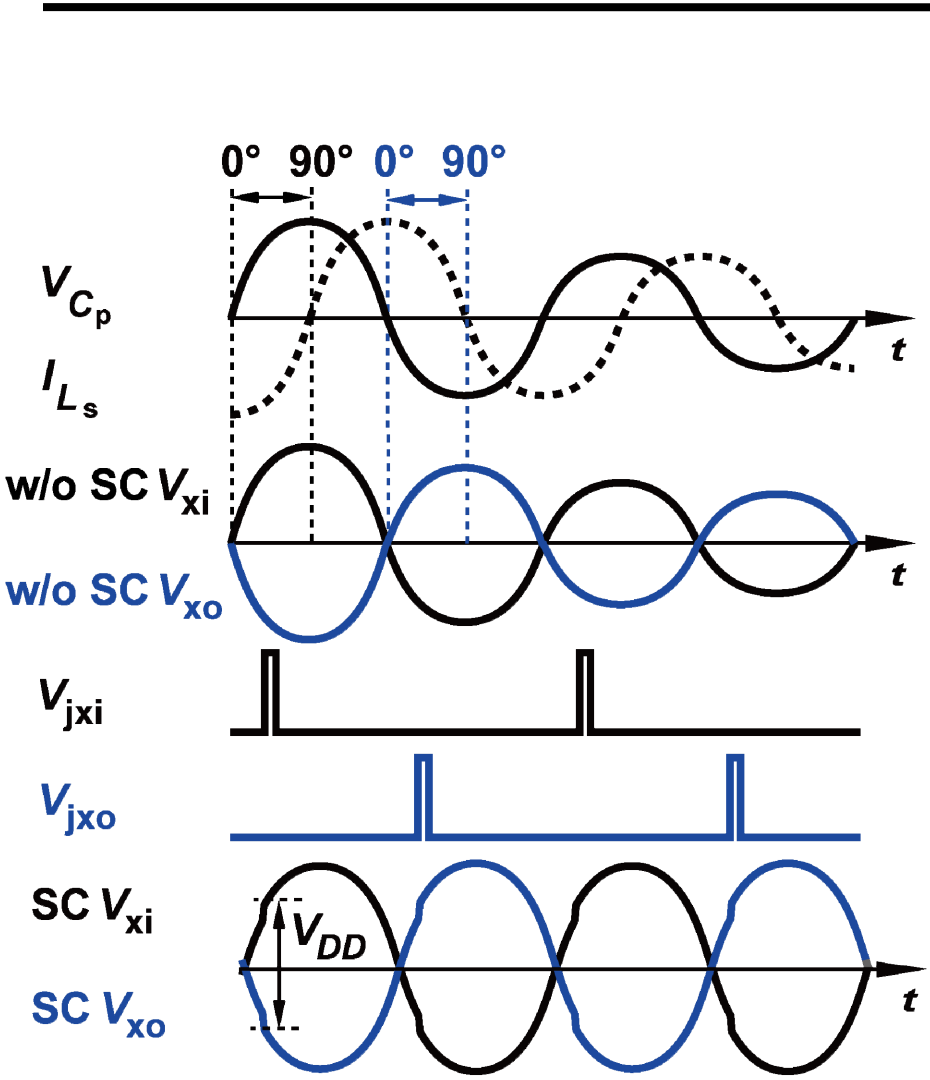
Example – A RTC XTAL

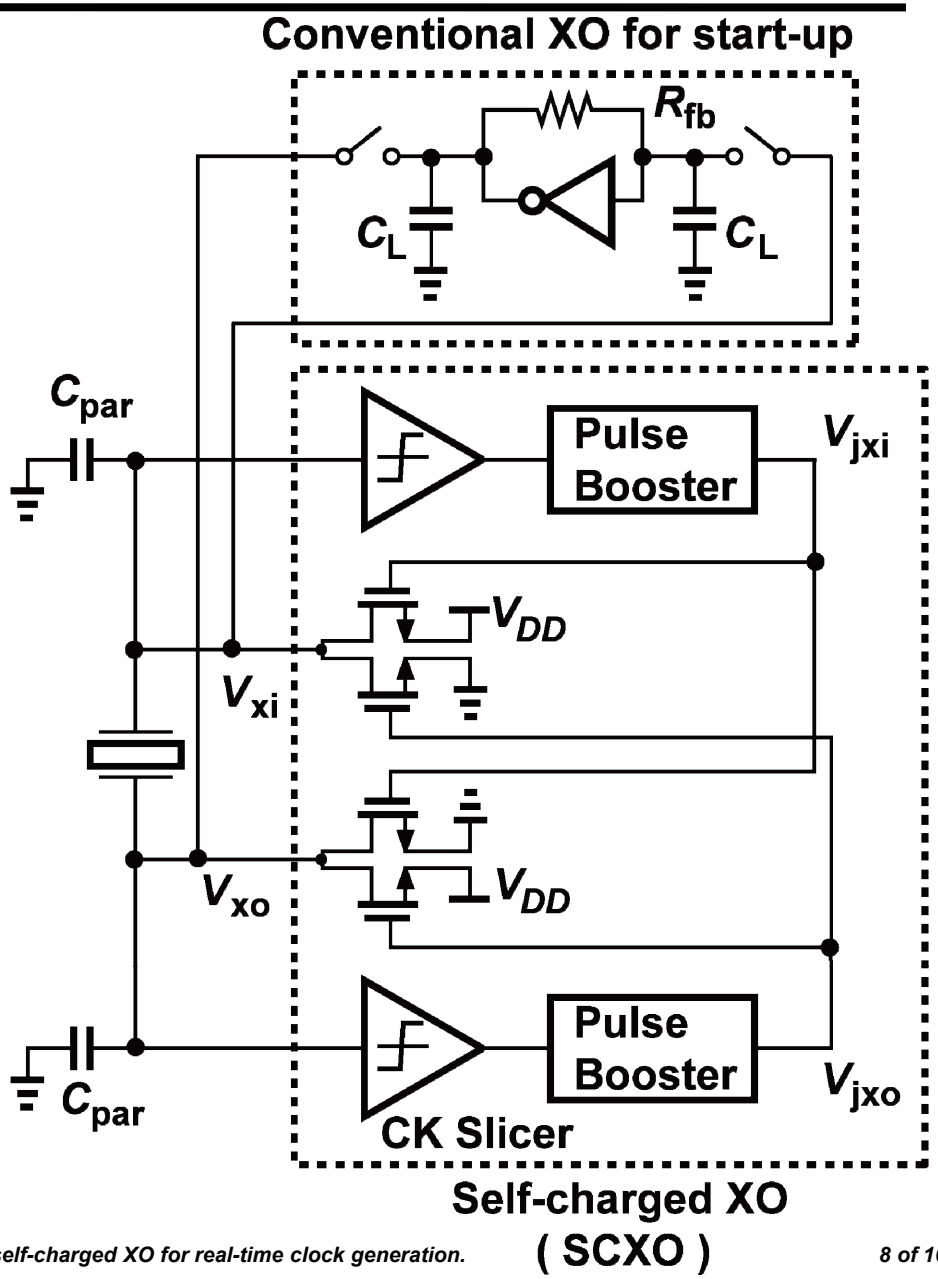
- L_s = 12.41886 kH
- C_s = 1.9 fF
- C_p = 0.8 pF
- R_s = 65 kΩ
- C_{par} = 3.3 pF
- V_{DD} = 200 mV



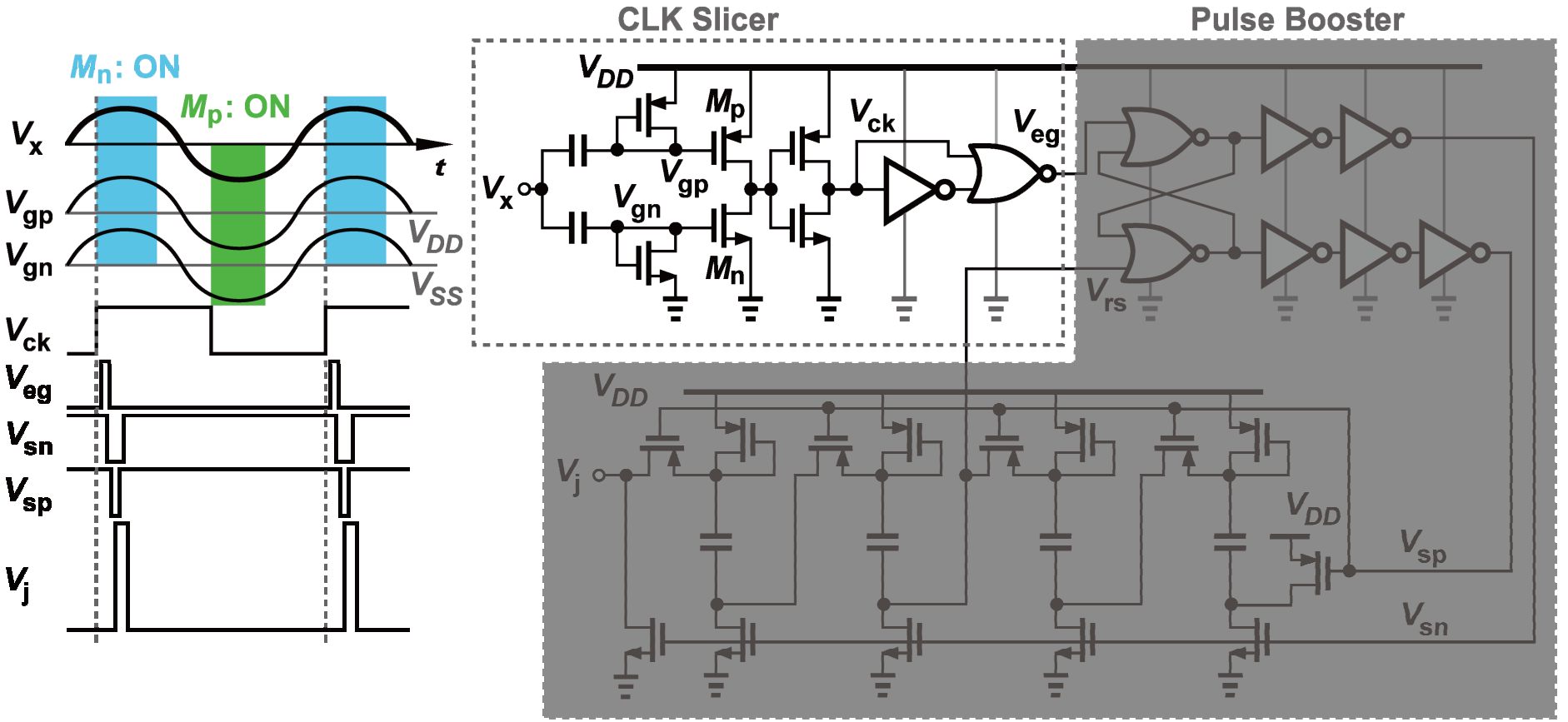
- V_{cp} = 172 mV
- $R_{s\text{-}pwr}$ = 0.33 nW
- Direct charging saves power!

Proposed Self-Charged XO (SCXO)



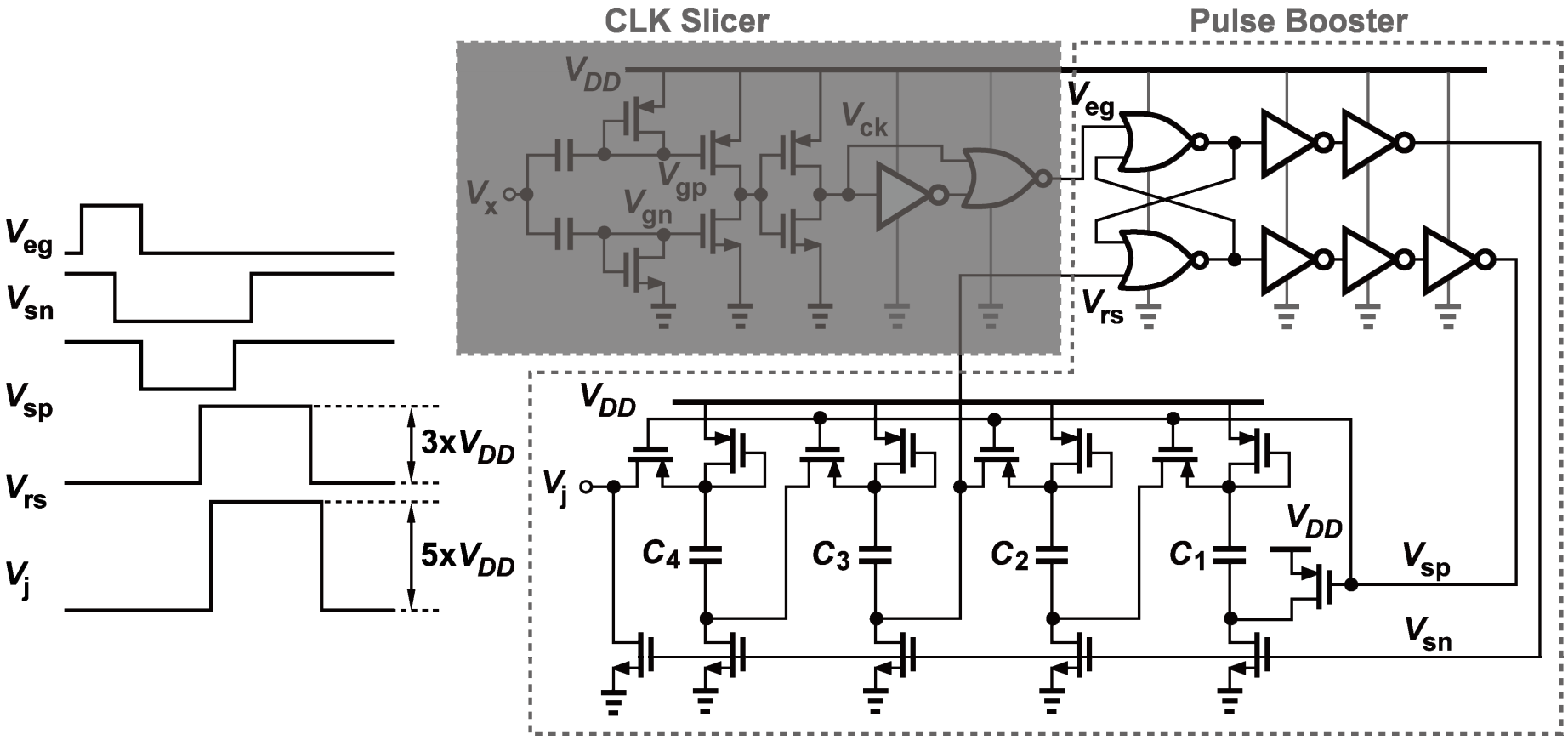


Schematic of the Clock Slicer



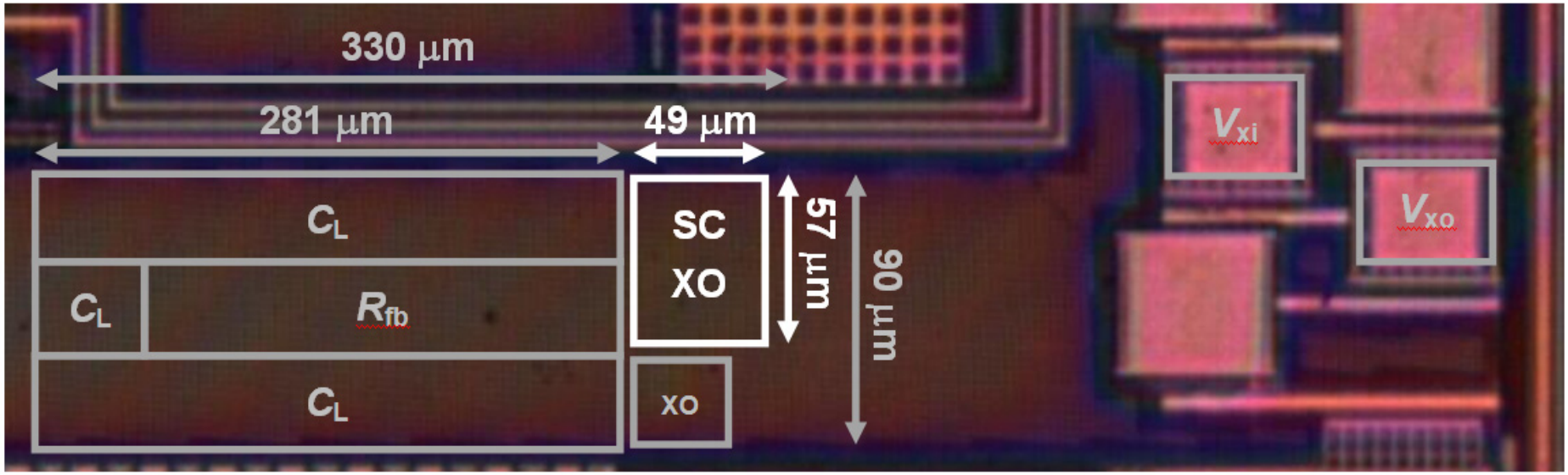
- **Dual-coupled structure boosts the clock slicer's power efficiency .**

Operation of the Pulse Booster



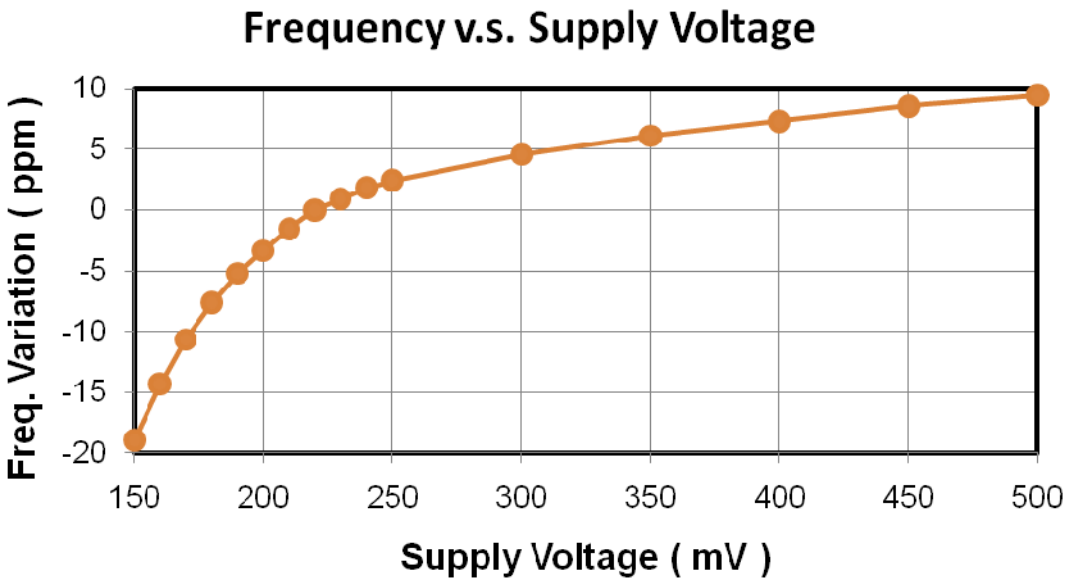
- **Pulse booster amplifies the voltage swing by 5 times.**

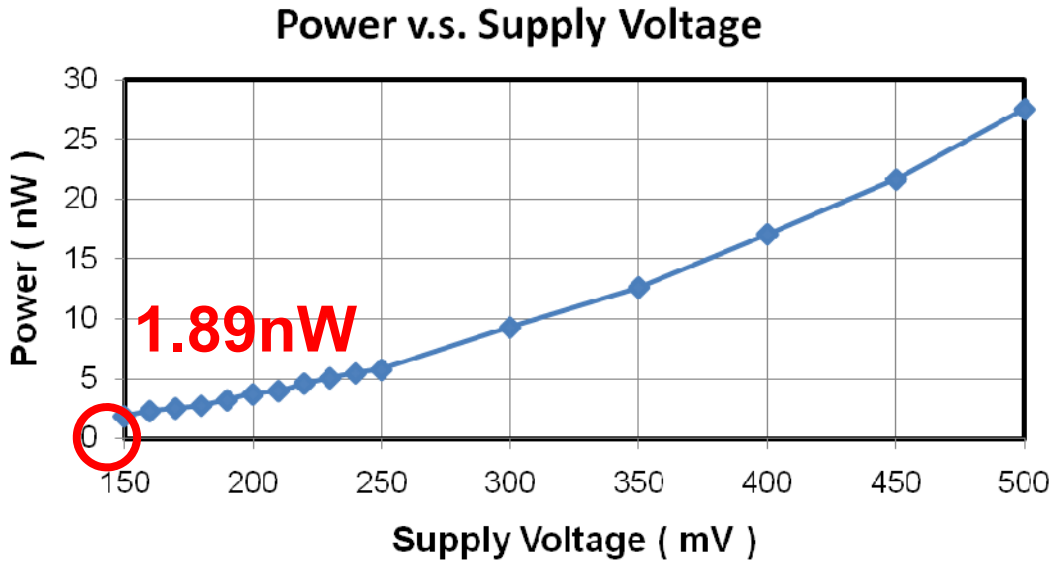
Die Photo



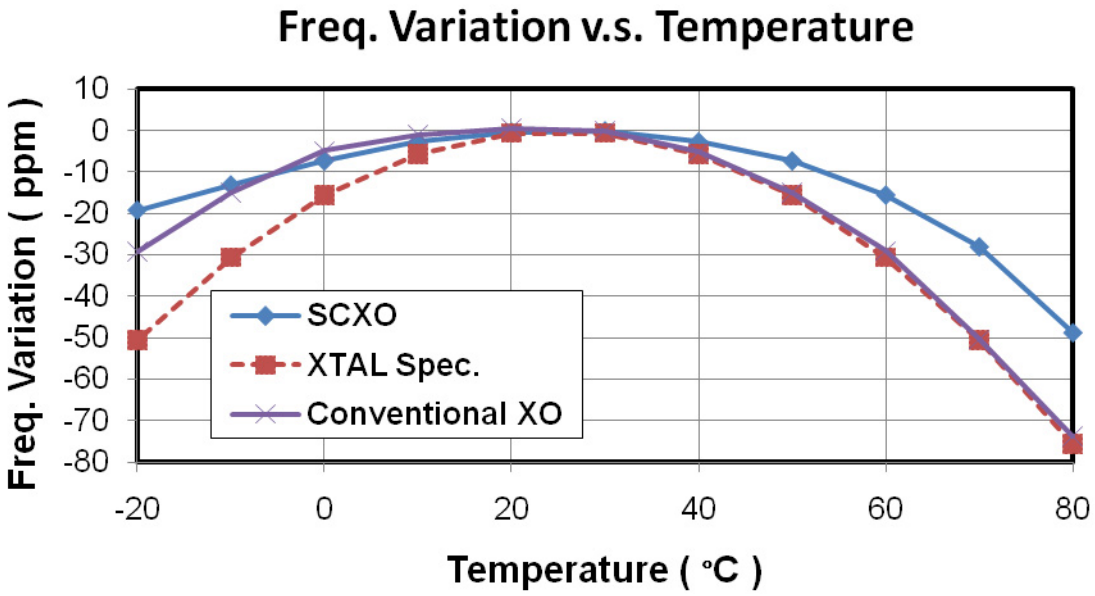
- Fabricated by TSMC 28 LP CMOS Process.
- Area of whole XO is 30000 μm^2.
- Area of the SCXO is 2600 μm^2.

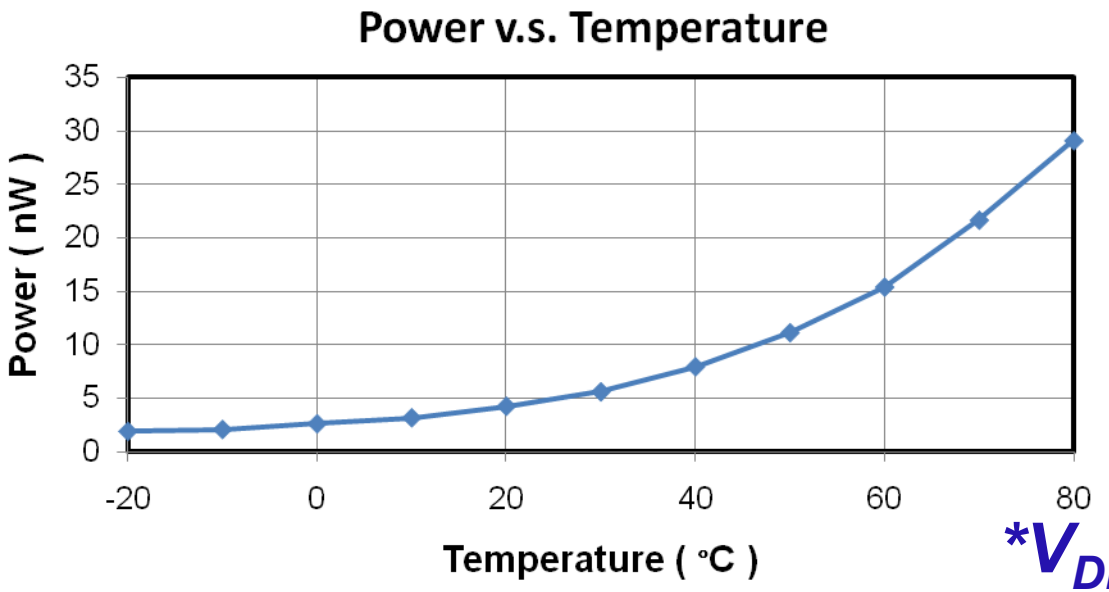
Freq. & Power v.s. Supply Voltage





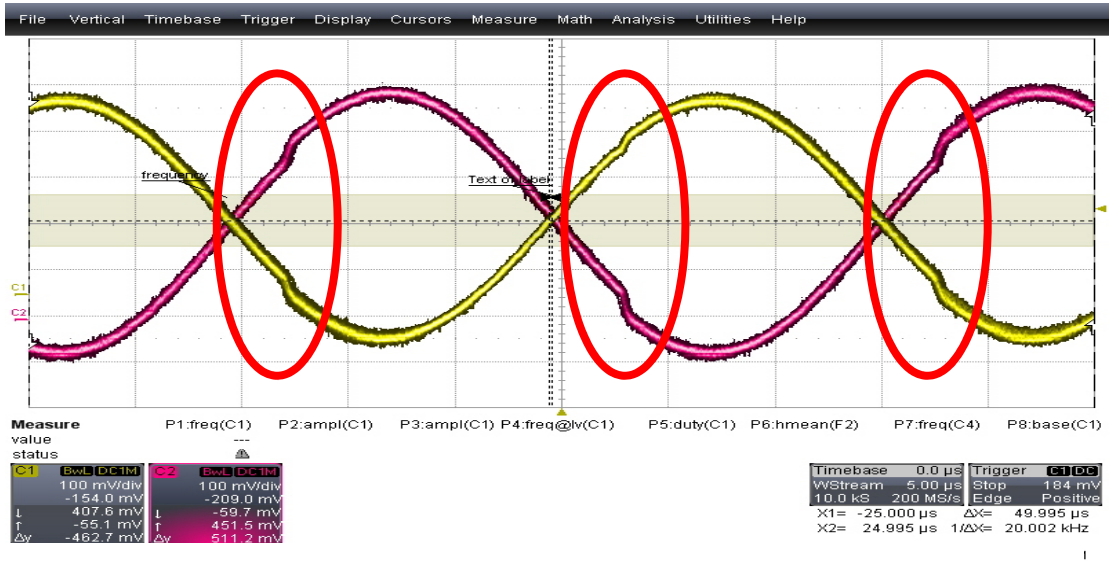
Freq. & Power v.s. Temperature

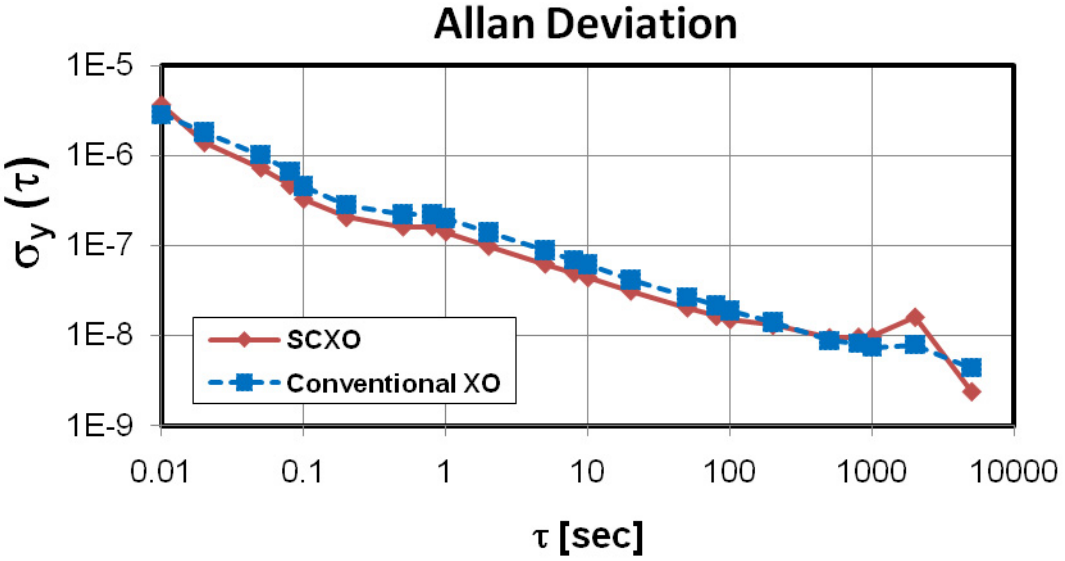




*V_{DD} = 250mV

Xi/Xo Waveform & Allan's Dev.





Performance Comparison

	Micro Crystal RV-2123-C2	ISSCC '94	ESSCIRC '99	ISSCC '12	This Work
Process	-	2 μm	2 μm	0.18 μm	**28 nm**
Area [mm^2]	-	-	-	0.3	**0.03**
Frequency [Hz]	32.768k	32.768k	32.768k	32.768k	**32.768k**
Min. Power [nW]	110	220	27	5.58	**1.89**
Supply Voltage [V]	1.1 - 5.5	1.1 – 2.2	1.2	0.92 – 1.8	**0.15 – 0.5**
Temperature Range [°C]	-40 - 85	-10 - 70	-	-20 - 80	**-20 - 80**
Freq. variation with Temp. [ppm]	147 @ -40~85°C	24 @ 0~50°C	-	133.3 @ -20~80°C	**48.8 @ -20~80°C**

Conclusion

- **A self-charged crystal oscillator is proposed and realized.**
- **The SCXO consumes only 1.89nW under 0.15V supply.**
- **Logic intensive design enables low-power and low-supply operation.**

A 190nW 33kHz RC Oscillator with ±0.21% Temperature Stability and 4ppm Long-Term Stability

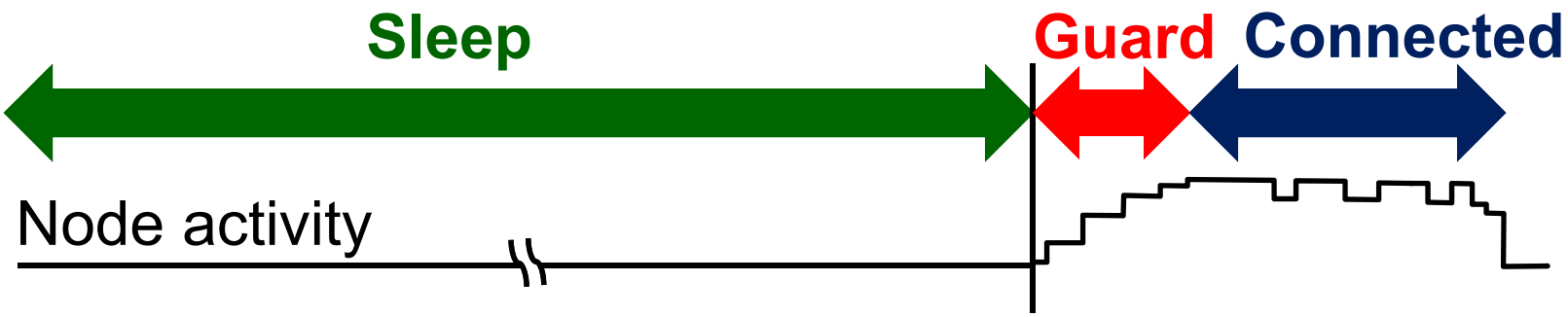
Danielle Griffith[1], Per Torstein Røine[2], James Murdock[1], Ryan Smith[1]

[1]Texas Instruments, Dallas, TX

[2]Texas Instruments, Oslo, Norway

ISSCC 2014

Sleep Timers in Wireless Systems



- Timer adds to **Sleep** power
- Accuracy determines Guard time duration

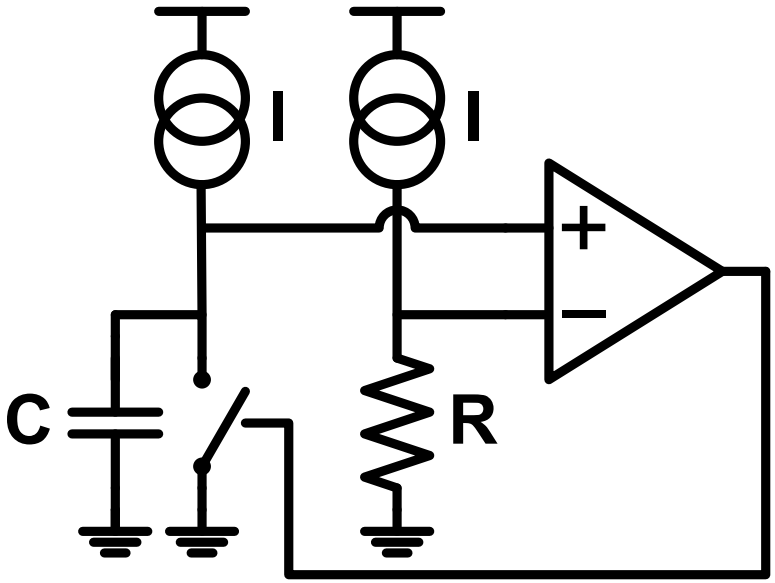
RF circuits are on in **Guard** time

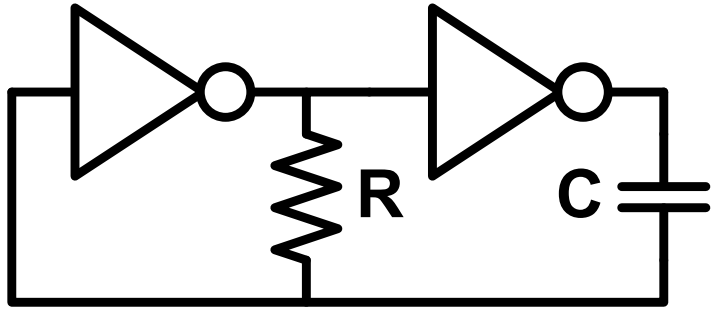
Useful TX/RX operation in **Connected** state

Sleep timer power-accuracy tradeoff

What alternatives are there to using low frequency crystal oscillators as a sleep timer?

Types of RC Oscillators

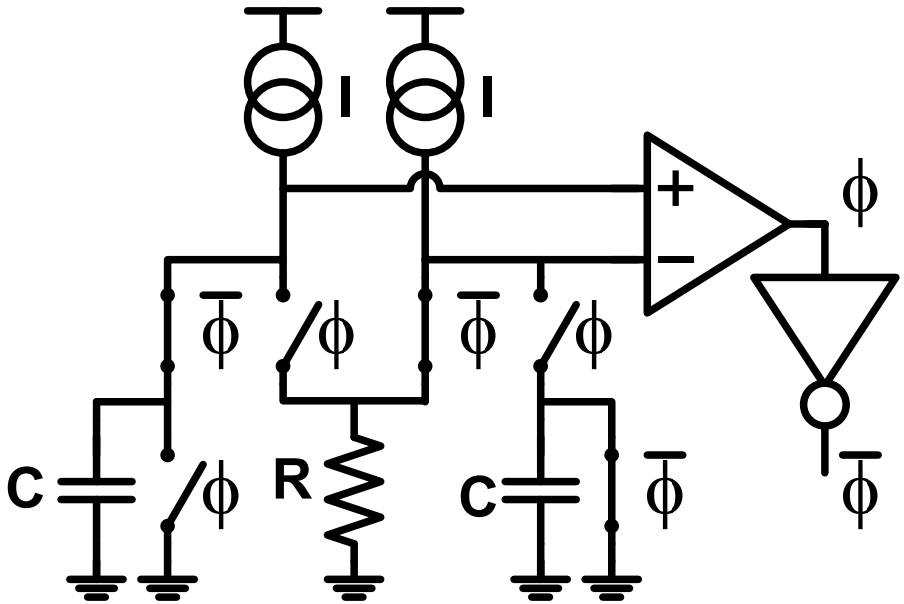




Frequency stability limited by noise/temperature/supply induced variations in:

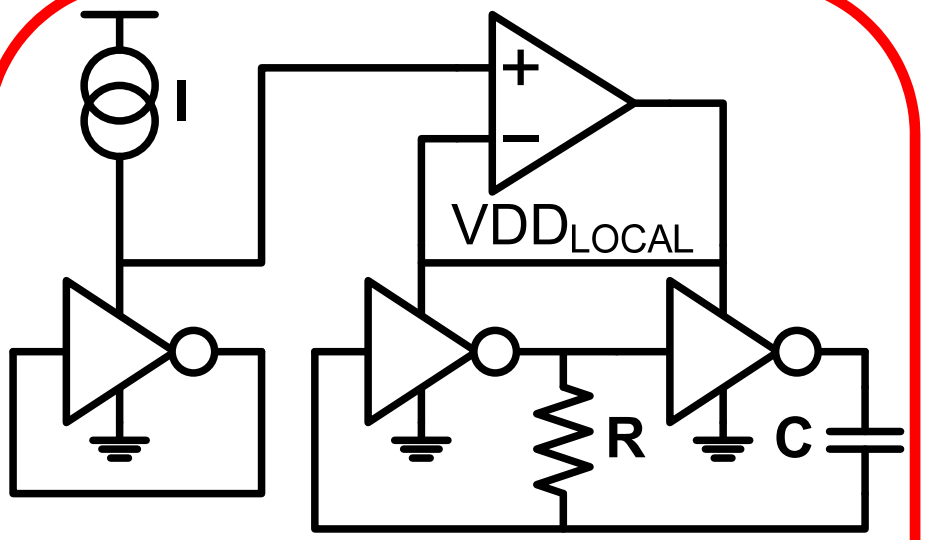
- Current mismatch
- Comparator offset
- Comparator delay
- Inverter delay

RC Oscillator Improvements



(ISSCC'13 [3])

- Chopping cancels offset & mismatch
- Still sensitive to delay variation

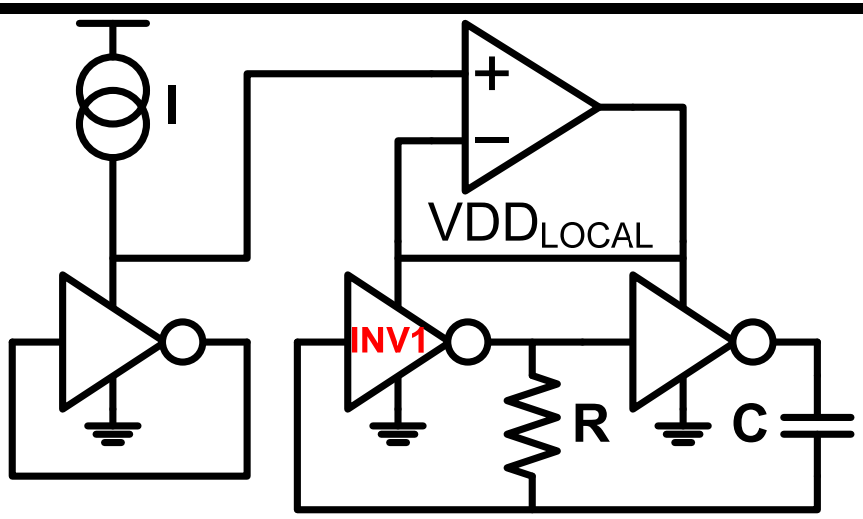


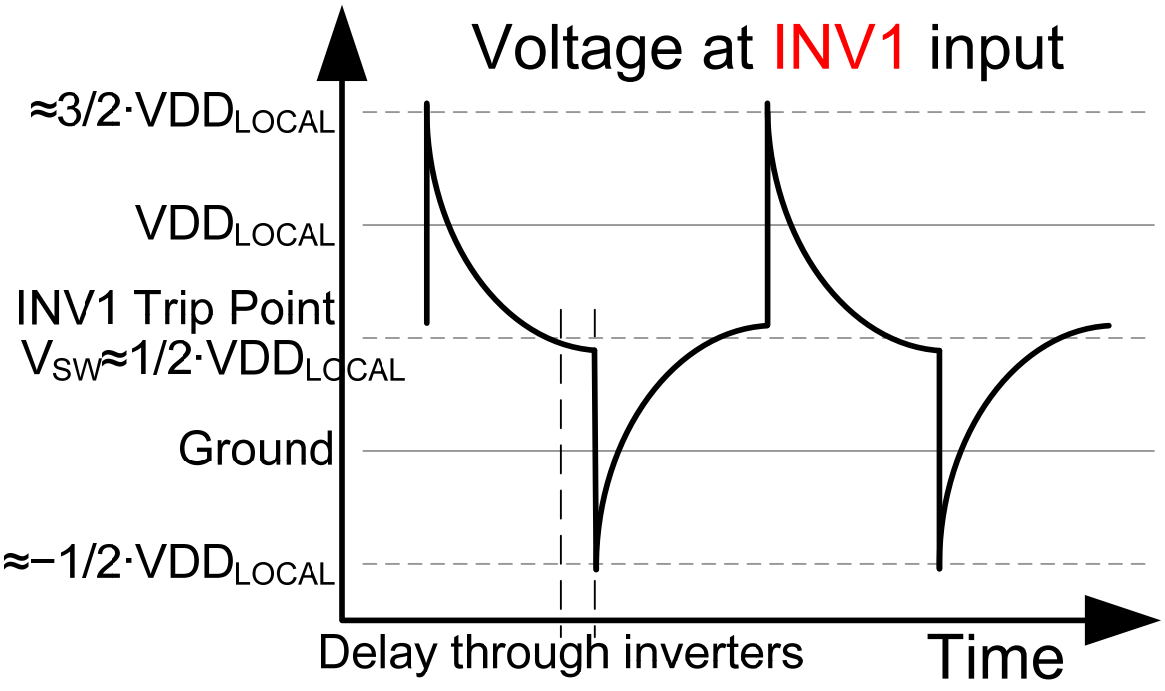
(This work)

- Local supply tracks inverter parameters
- Delay varies less with supply & temperature

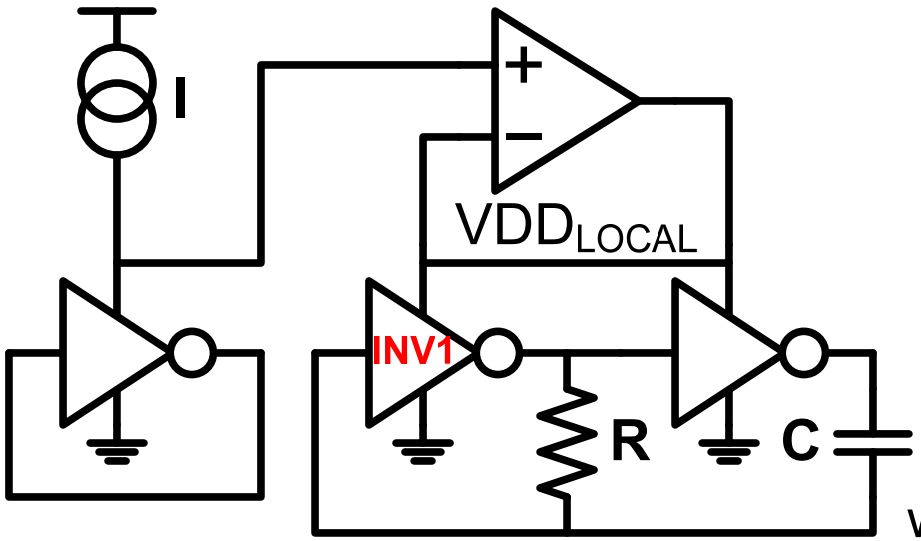
Supply Tracking RC Oscillator

- Constant inverter delay over supply and temperature
- VDD_{LOCAL} supply tracks threshold voltage variation
- Low power by sub-threshold operation ($VDD_{LOCAL} \approx 0.65V$)
- Positive & negative capacitor charging halves cap area for a given frequency





Oscillator Frequency Sensitivity



$$K_{SW} = \frac{V_{SW}}{VDD_{LOCAL}}$$

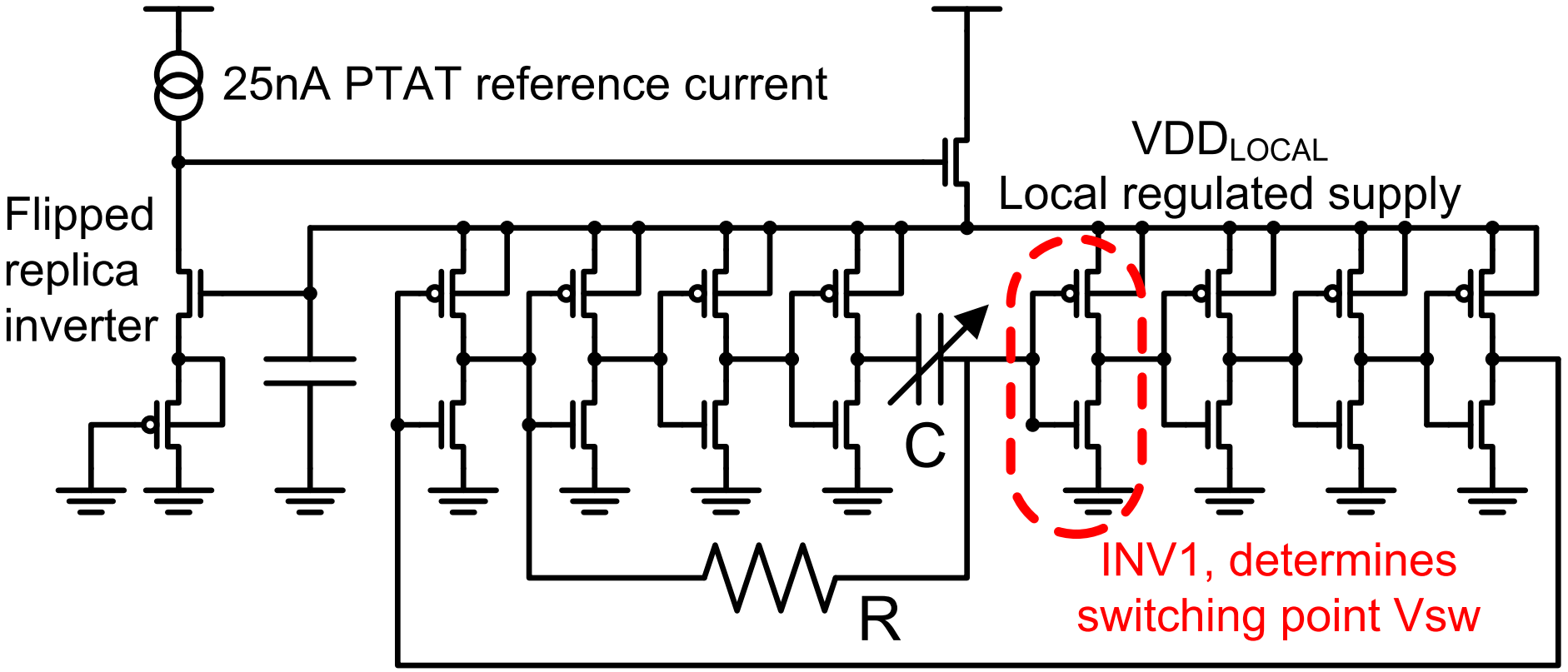
$$t_0 = RC \ln\left(\frac{(1+K_{SW})(2-K_{SW})}{(K_{SW})(1-K_{SW})}\right)$$

when $K_{SW} = 0.5 \rightarrow t_0 \approx 2.2 \cdot RC$

(neglecting inverter delay)

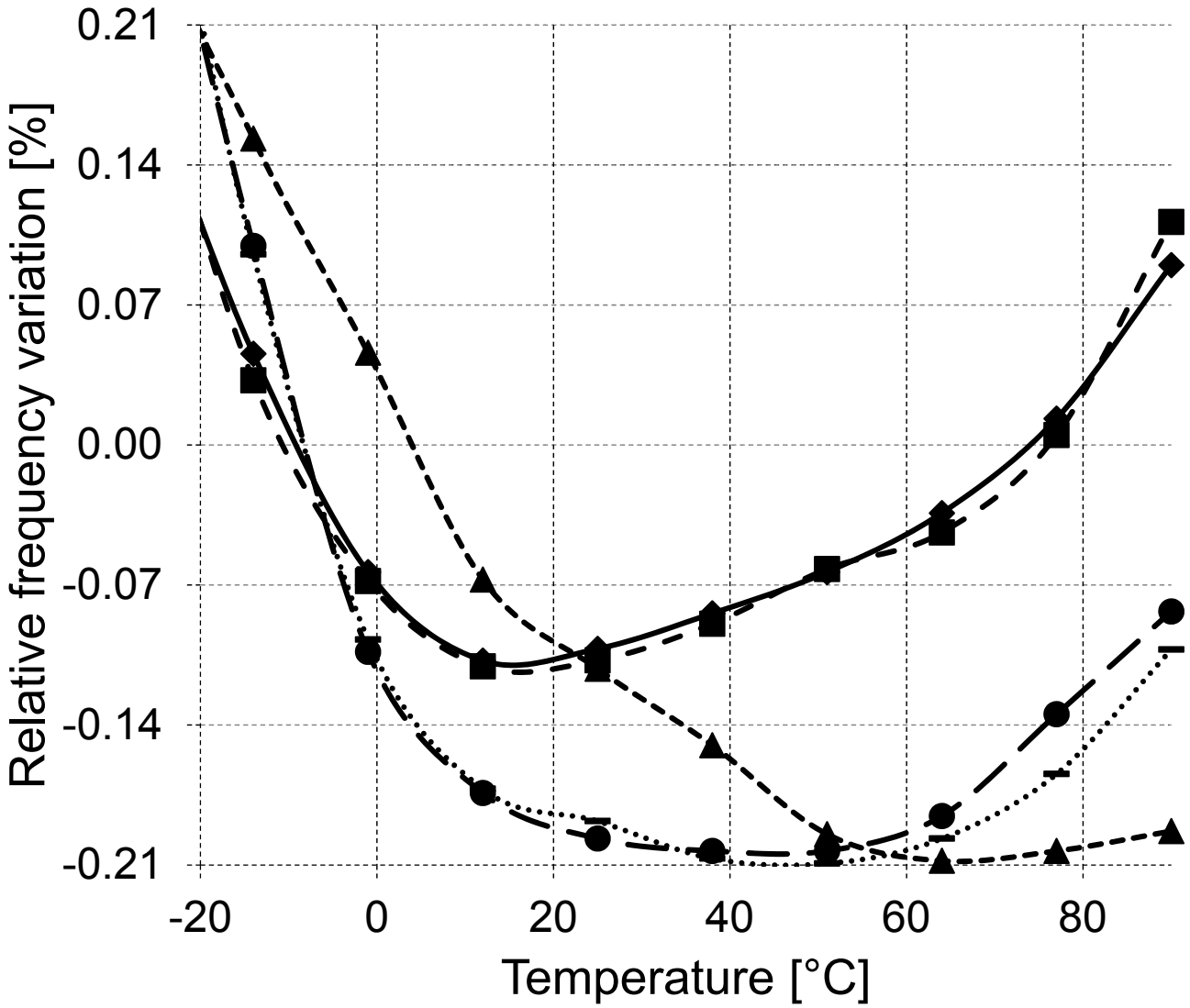
- Noise in INV1 results in K_{SW} variation
- Rising and falling edges affected almost equally, so period almost constant
- K_{SW}=0.45 gives 53%/47% duty cycle, but only 0.4% change in oscillation period.

RC Oscillator Implementation



- Zero temperature coefficient resistor
- Metal finger capacitor array for frequency tuning
- Multiple inverters to ensure a square wave

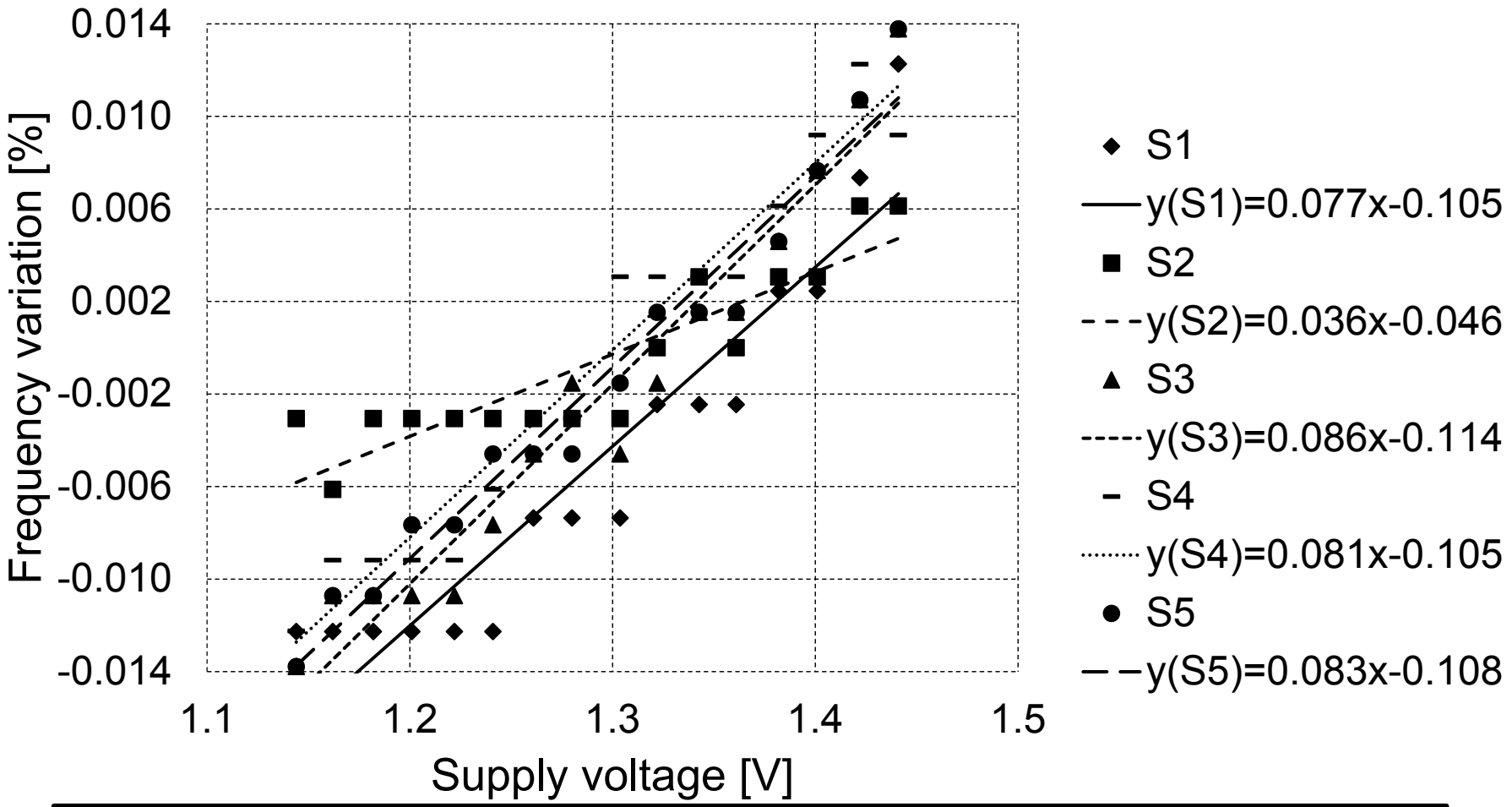
Temperature Stability of ±0.21%



after 1 time frequency trim at room temperature

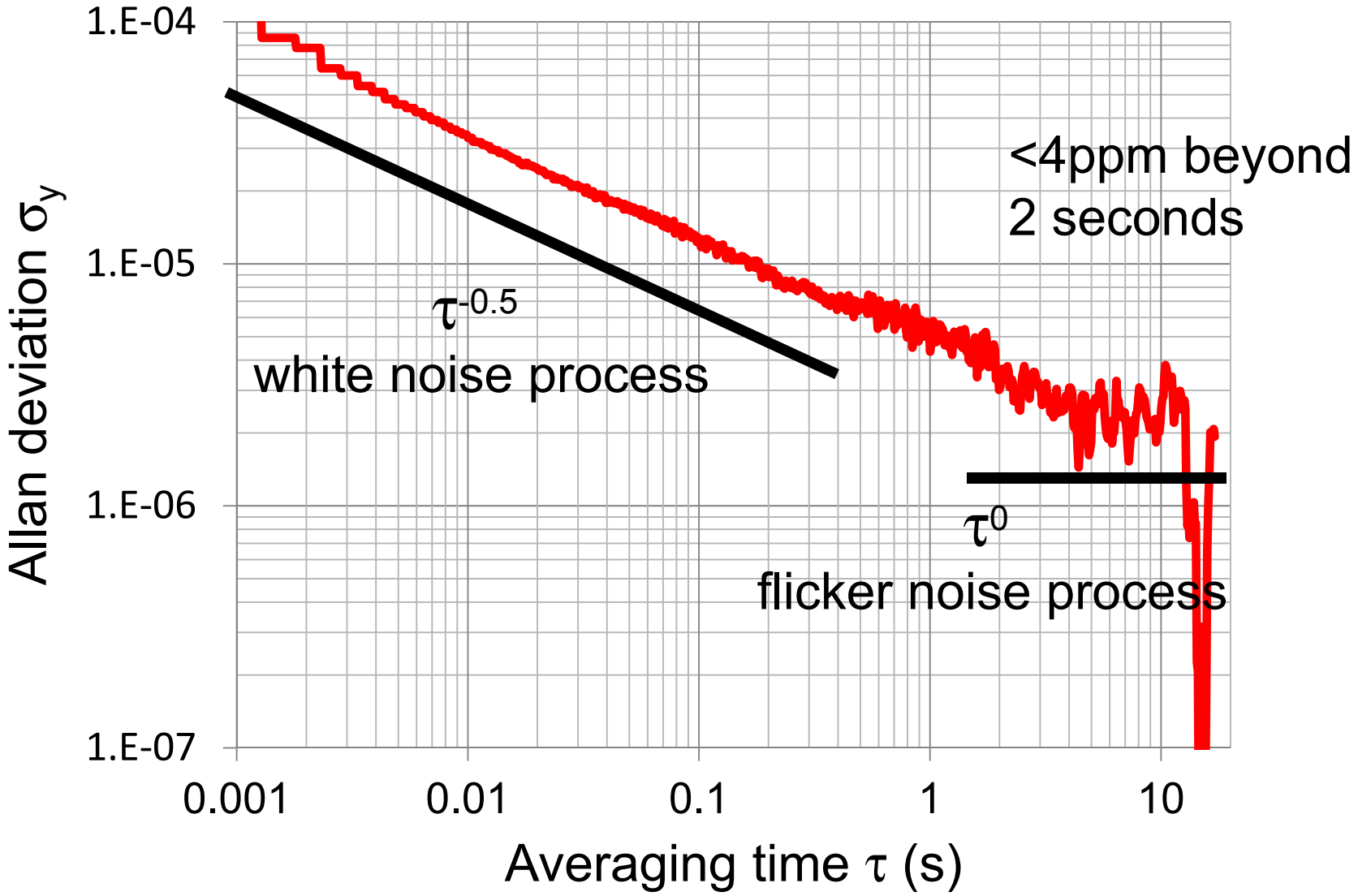
- S1, 33884Hz
- S2, 32857Hz
- S3, 32442Hz
- S4, 32206Hz
- S5, 32127Hz

Supply Sensitivity of 0.09%/V

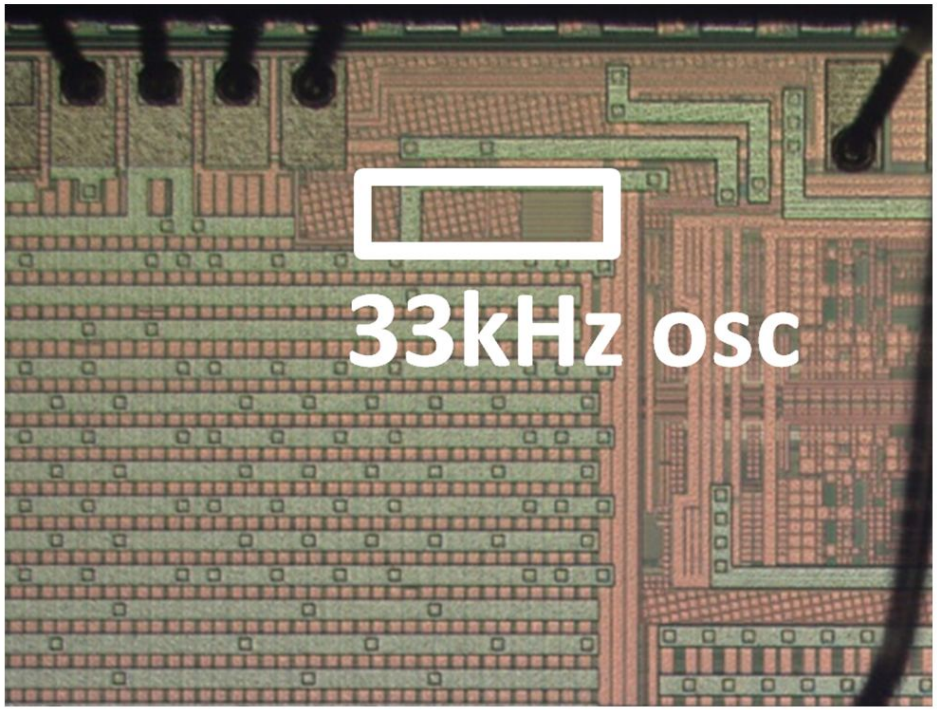


Operating the oscillator from VDD_{LOCAL} allows stable frequency with voltage.

Long Term Stability of 4ppm



Performance Summary



65nm CMOS

Area	0.015 mm^2
Voltage	1.25V
Frequency	33 kHz (nom.)
Tuning	13 kHz – 248 kHz
Supply Sensitivity	< 0.09%/V
Temp. Stability	±0.21% (−20 to +90°C)
Allan Deviation	4ppm beyond 2s
Power	190 nW (nom.)

kHz RC Oscillators Comparison

	[1] VLSI'12	[2] VLSI'12	[3] ISSCC'13		[5] JSSC'09	This work
Process	90nm	60nm	65nm		65nm	65nm
Area [mm^2]	0.12	0.048	0.032		0.11	0.015
Freq (kHz)	100	32.768	18.5		100	33
Power (μW)	0.28	4.48	0.12		20.8	0.19
Power/Freq (μW/MHz)	2.8	137	6.5		208	5.8
Temp Accuracy (%)	±0.68	±0.1	±0.25	±0.1	±1.1	±0.21
Temp Range (°C)	−40 to 90	−20 to 100	−40 to 90	0 to 90	−22 to 85	−20 to 90
Supply Sensitivity (%/V)	9.4	0.06	1		0.37	0.09
Allan Deviation Floor	N/A	N/A	< 20 ppm		≈1000ppm	< 4 ppm

Conclusions

- RC oscillator architecture enables ultra-low power consumption of 190nW
  - Inverter as a comparator for low power
  - Biased from a supply that tracks inverter characteristics for stable frequency
  - Rising and falling edges affected almost equally by noise and offsets, so frequency almost constant
  - Low area due to charging capacitor over 2x voltage
- Frequency stability of ±0.21% over −20 to +90°C
- Long term Allan deviation less than 4ppm

Acknowledgements

- S. Sundar, Texas Instruments

COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

A 0.6V 70MHz 4th Order Continuous-Time Butterworth Filter with 55.8dB SNR, 60dB THD at +2.8dBm Output Signal Power

Jayanth Kuppambatti, Baradwaj Vigraham and Peter Kinget

Analog & RF Design Research

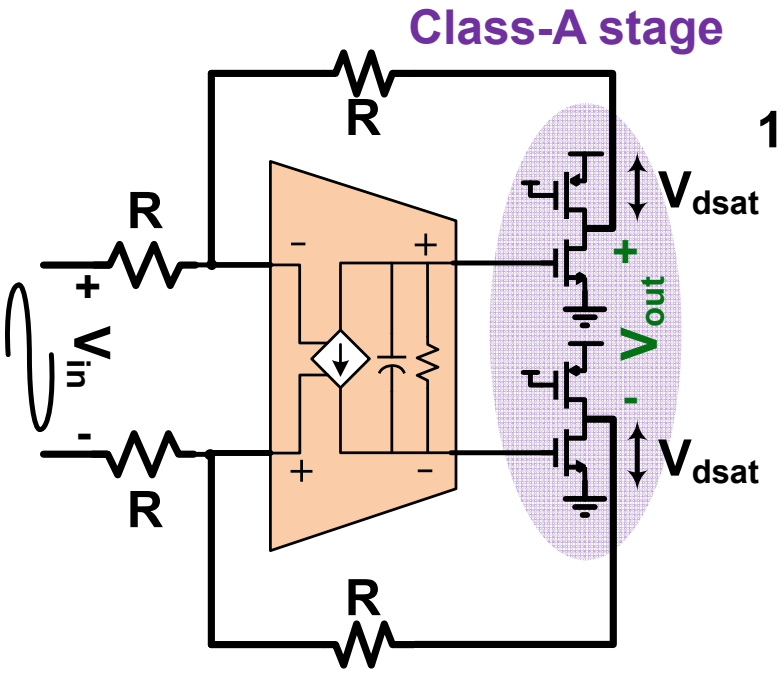
Columbia Integrated Systems Laboratory

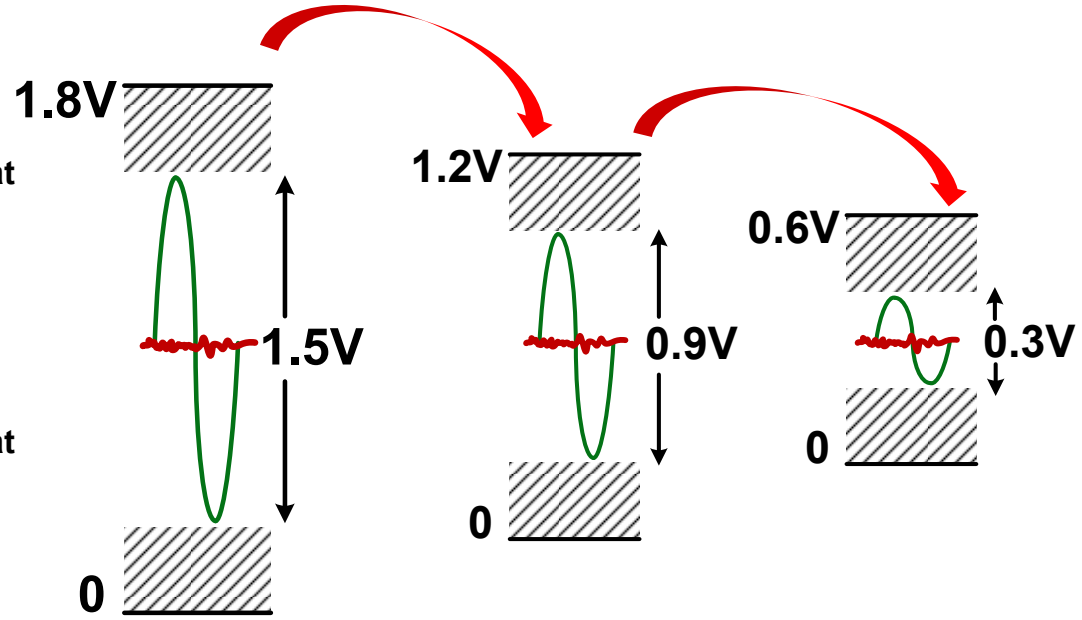
http://www.cisl.columbia.edu

Outline

- Motivation: Supply scaling
- Switched-mode operational amplifiers
- Continuous-time filter prototype
- Measurement results
- Conclusions

Analog Design in Scaled CMOS



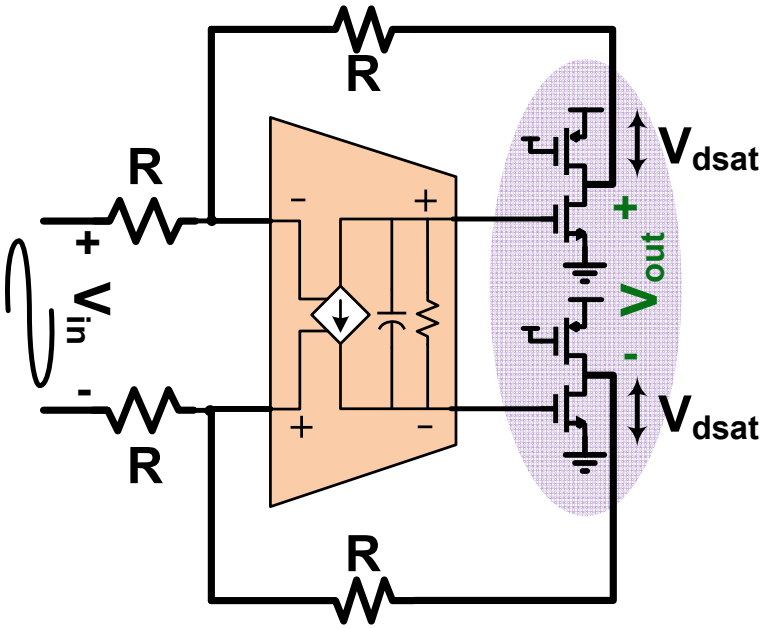


Output devices biased in saturation with $V_{dsat} \approx 150mV$

Supply V	1.8	1.2	0.6
Max P_{sig} dBm	7.5	3	-6

13.5dB loss

Effect of V_{dd} Scaling on Power

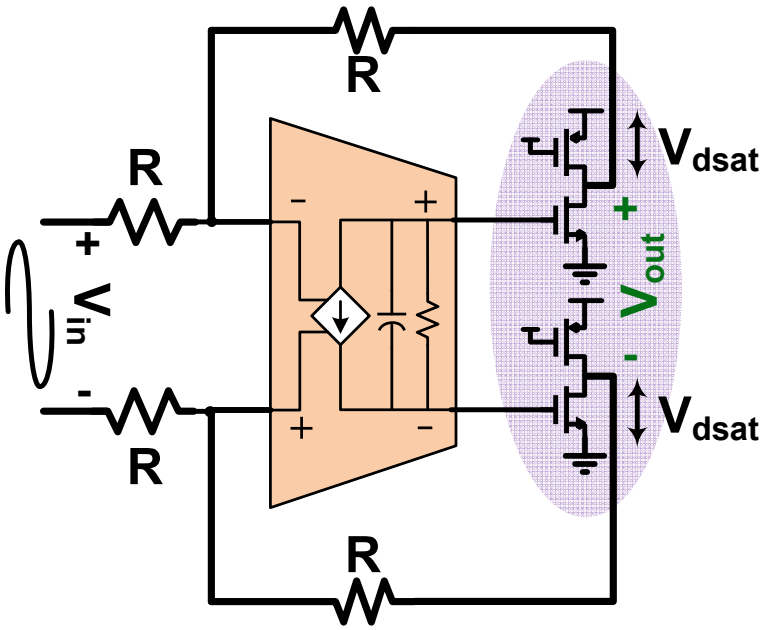


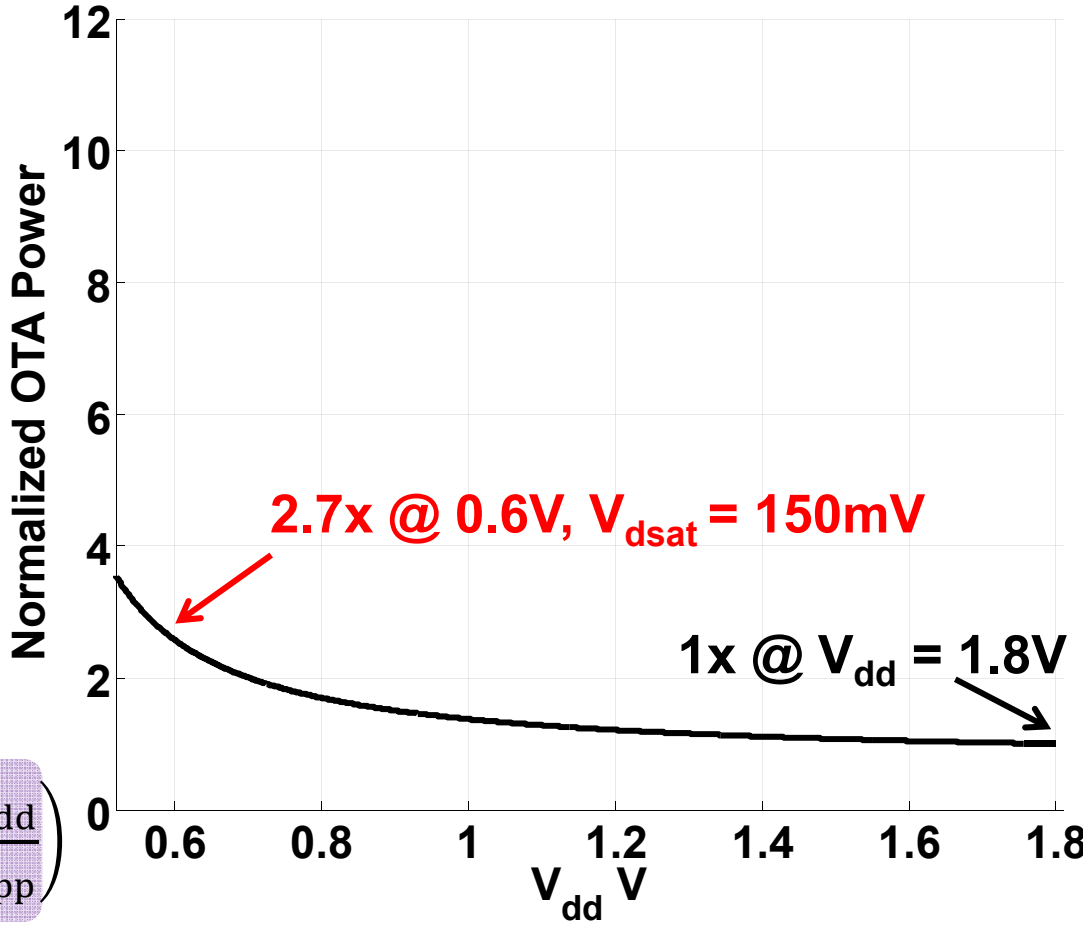
$$P_{OTA} = 4kTB \times SNR \times \left(\frac{\beta V_{dsat} V_{dd}}{V_{pp}^2} + \frac{\alpha V_{dd}}{\eta V_{pp}} \right)$$

Noise limited at low V_{dd}

Output η limited at high V_{dd}

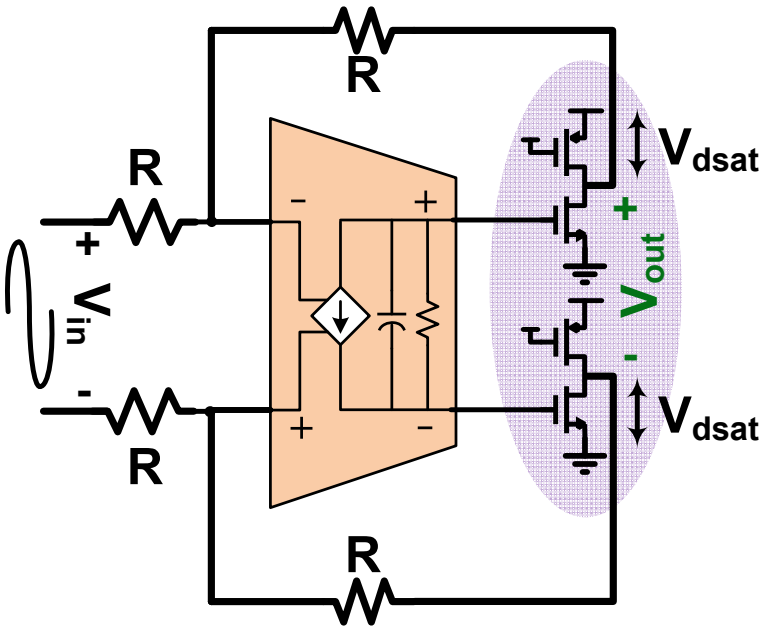
Effect of V_{dd} Scaling on Power

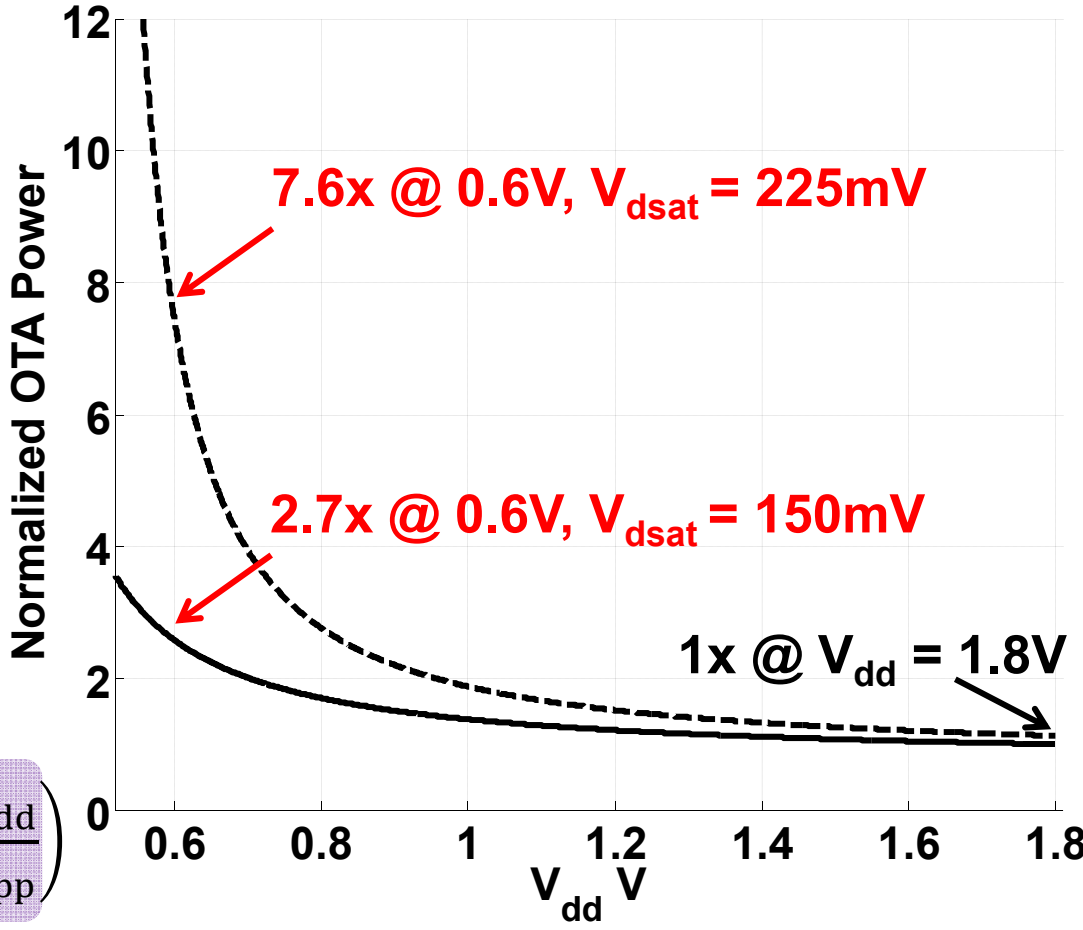




$$P_{OTA} = 4kTB \times SNR \times \left(\frac{\beta V_{dsat} V_{dd}}{V_{pp}^2} + \frac{\alpha V_{dd}}{\eta V_{pp}} \right)$$

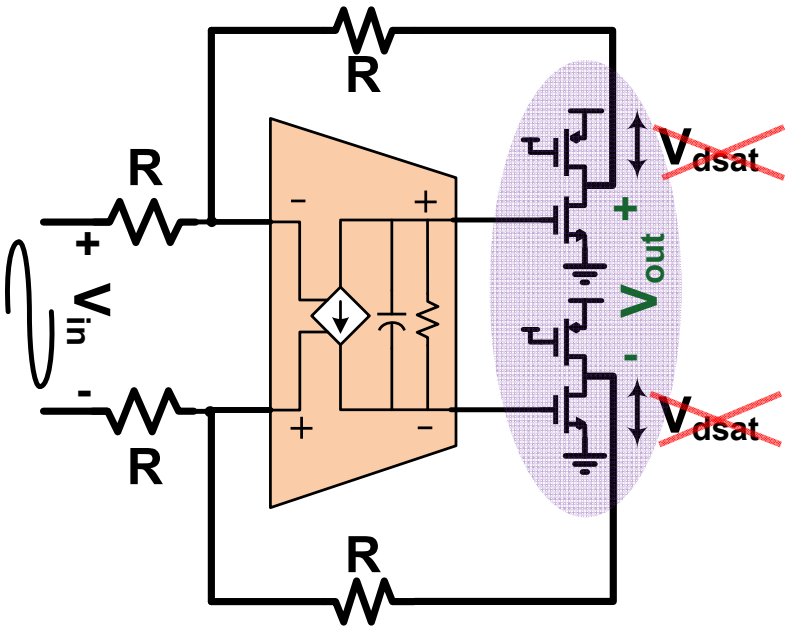
Effect of V_{dd} Scaling on Power

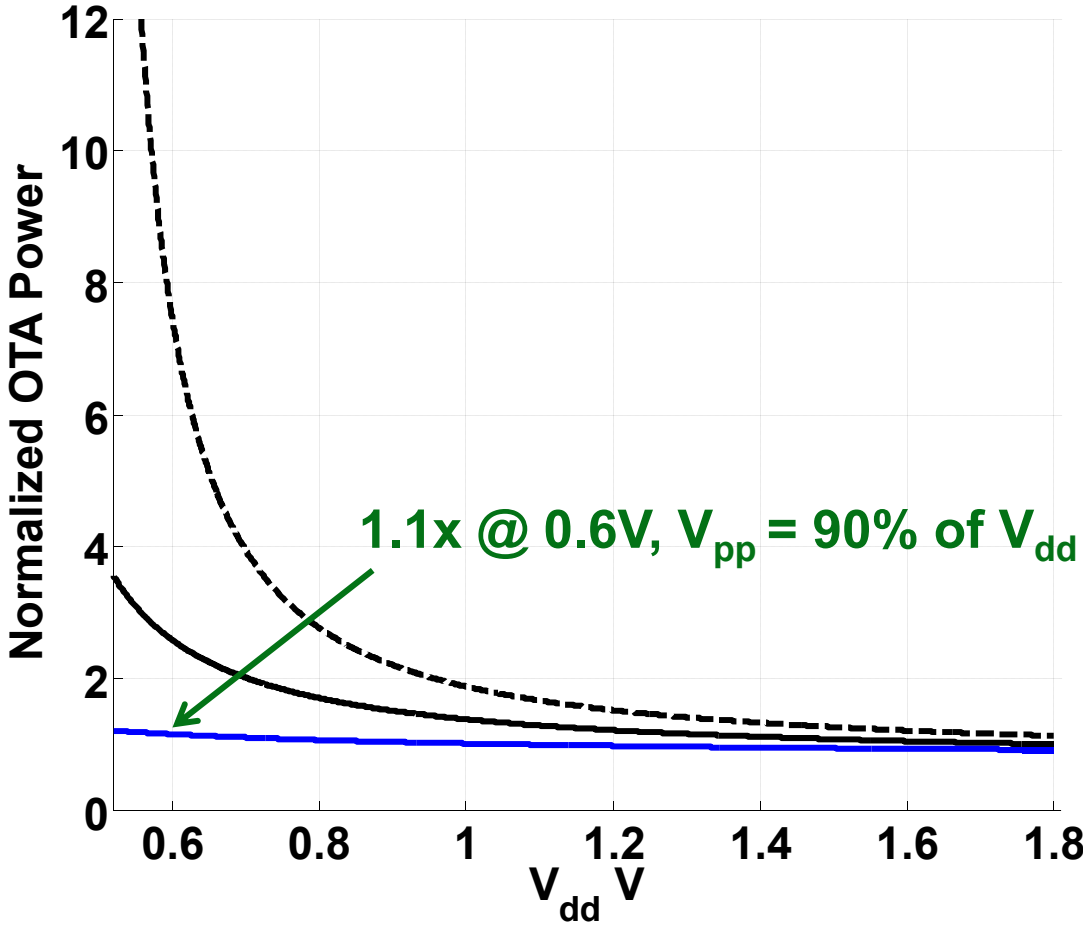




$$P_{OTA} = 4kTB \times SNR \times \left(\frac{\beta V_{dsat} V_{dd}}{V_{pp}^2} + \frac{\alpha V_{dd}}{\eta V_{pp}} \right)$$

Power with Rail-to-Rail Swing

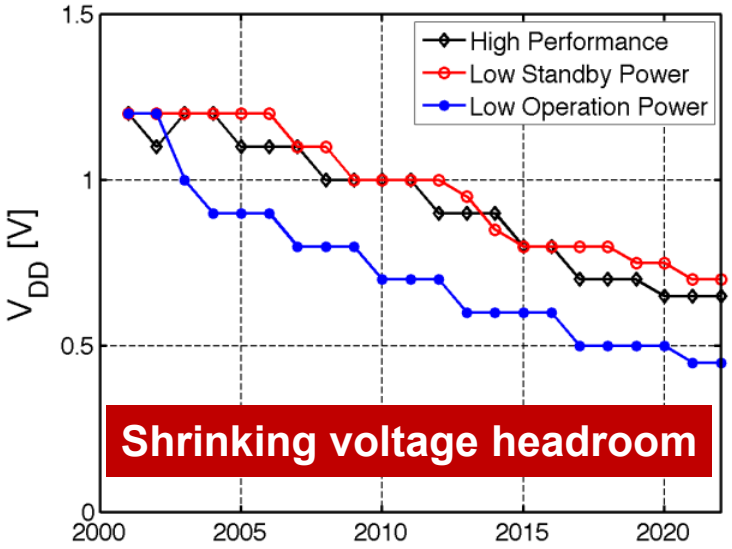


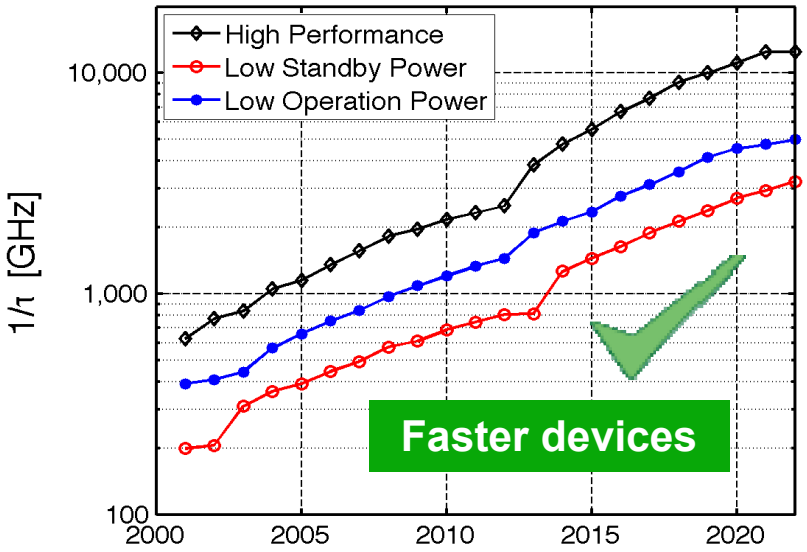


How do we achieve rail-to-rail swings in amplifiers at low V_{dd}???

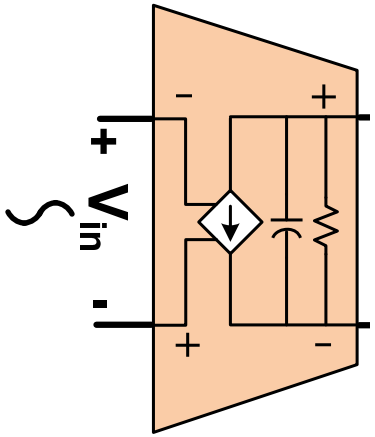
Leveraging Faster Devices

Voltage-based Architectures	Time and phase-based Architectures

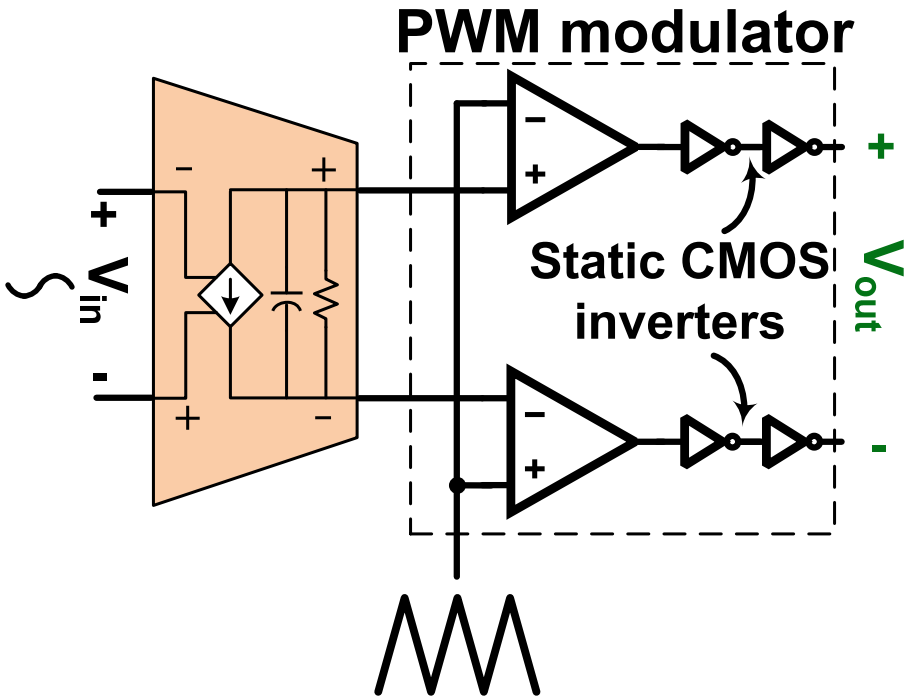


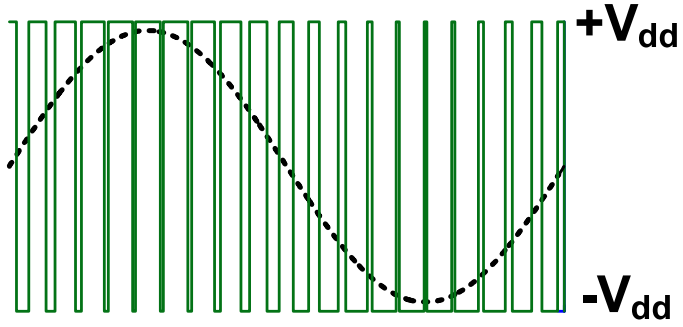


Switched-Mode Operational Amplifier



SMOA Rail-to-Rail Signal Swing



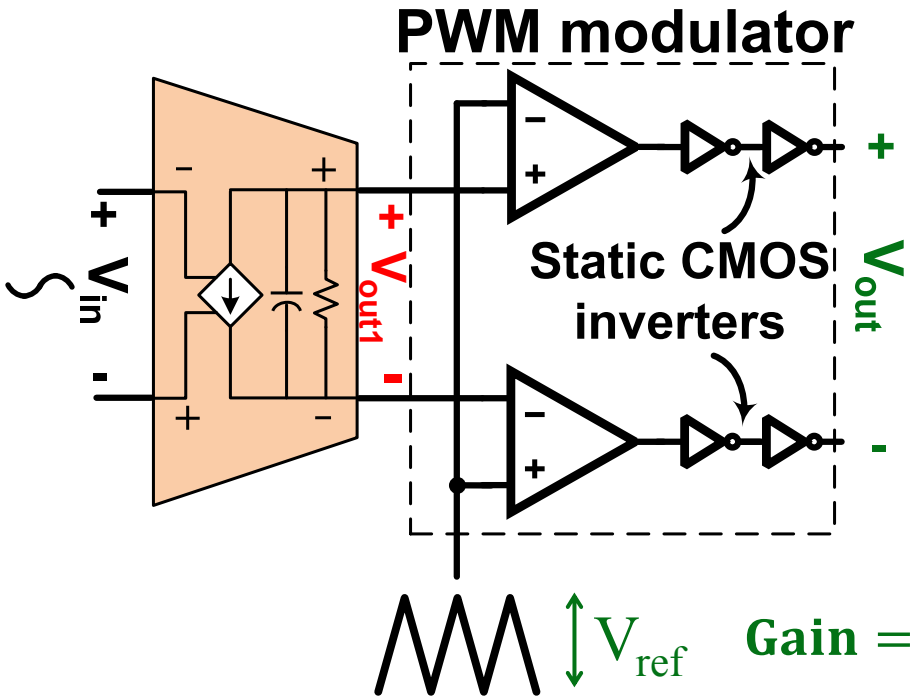


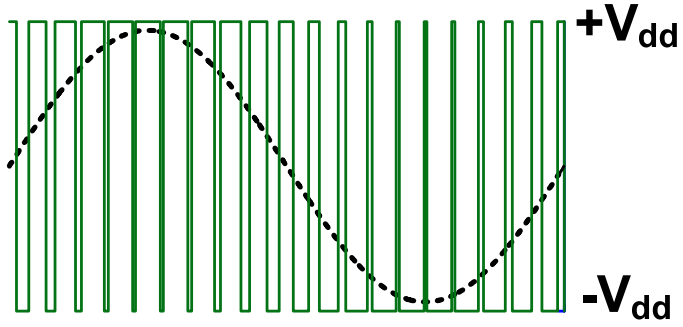
$$V_{pp} = V_{dd}\,(1-2t_{min}F_{PWM})$$

t_{min} = 150ps, F_{PWM} = 300MHz $\Rightarrow$ V_{pp} = 91% of V_{dd} @ 0.6V

V_{pp} improves with technology scaling ☺

SMOA Output Stage Gain



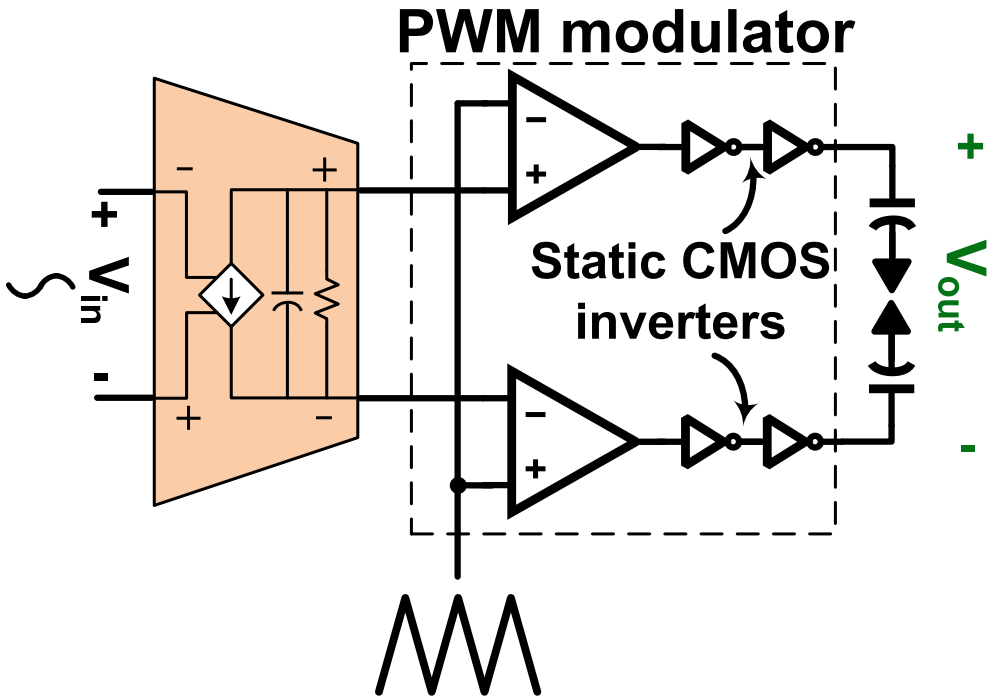


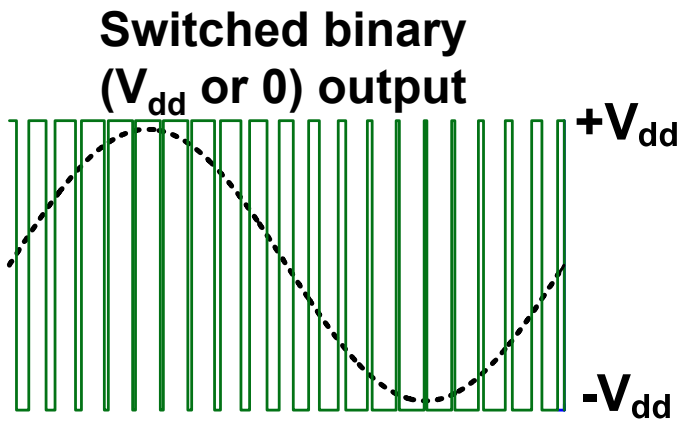
$$\text{Gain} = \frac{2V_{dd}}{V_{ref}} \approx 4$$

PWM stage gain reduces signal swing at V_{out1}

V_{out} swings $\pm 0.6V \Rightarrow V_{out1}$ swings only $\pm 0.15V$

Load-independent SMOA Bandwidth



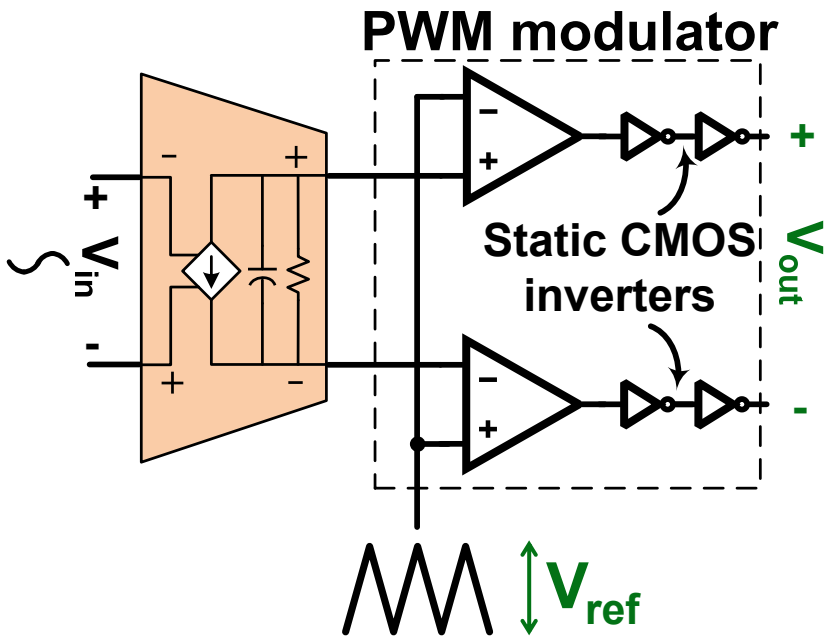


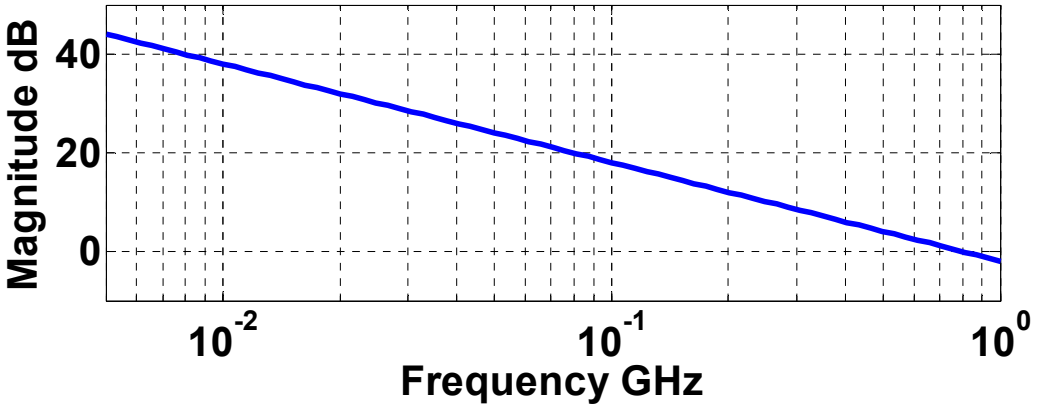
Low *open-loop* output impedance

⇒ True *operational* amplifier

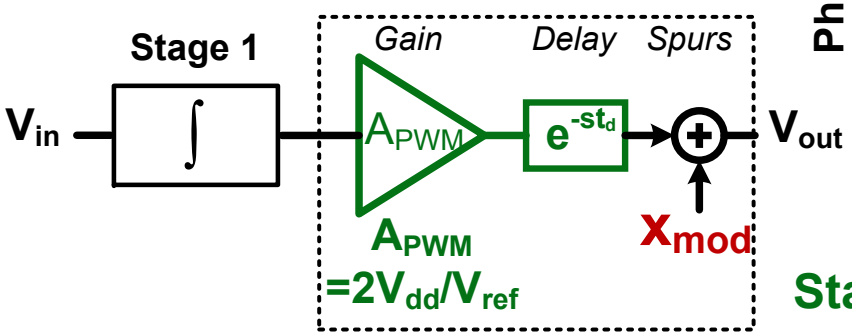
Output loading does not affect SMOA bandwidth ☺

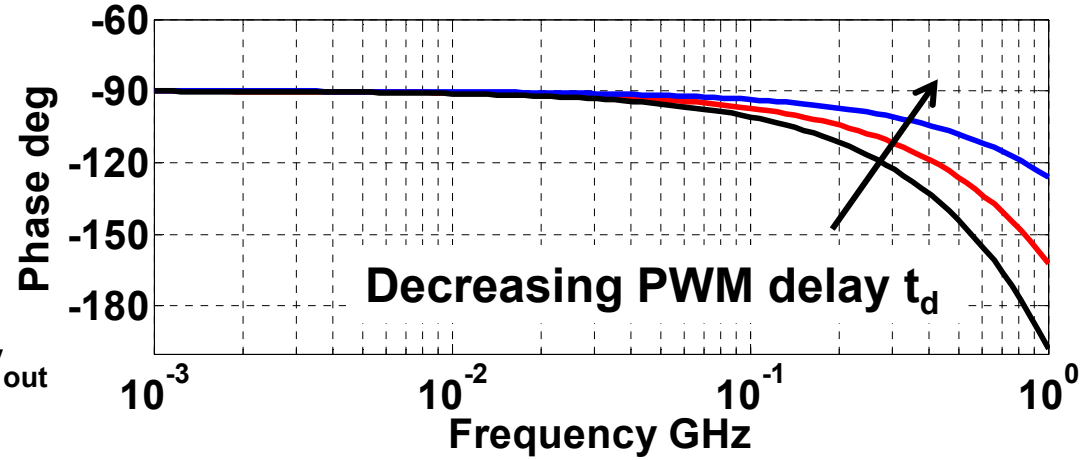
SMOA Model





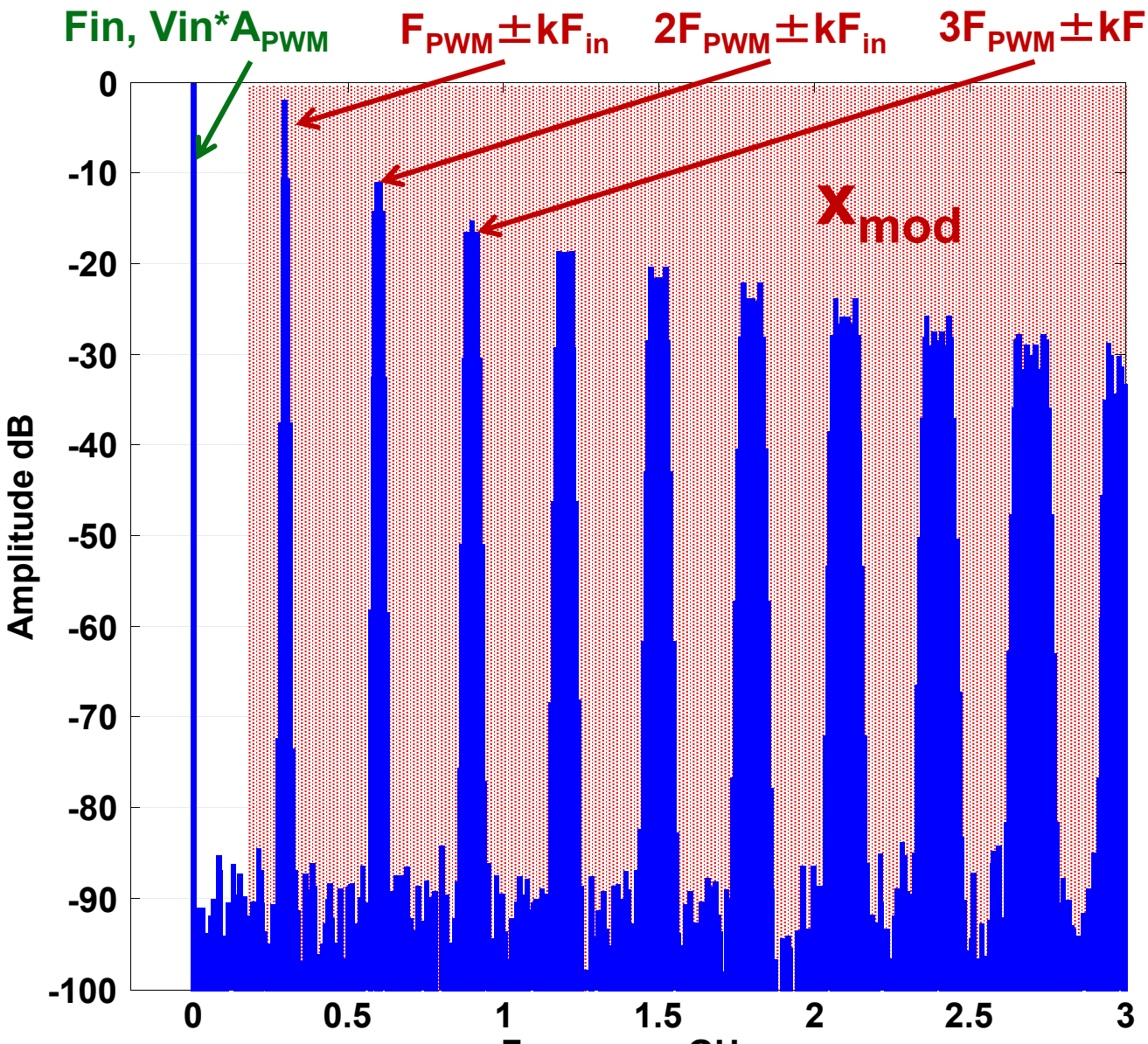
PWM Modulator





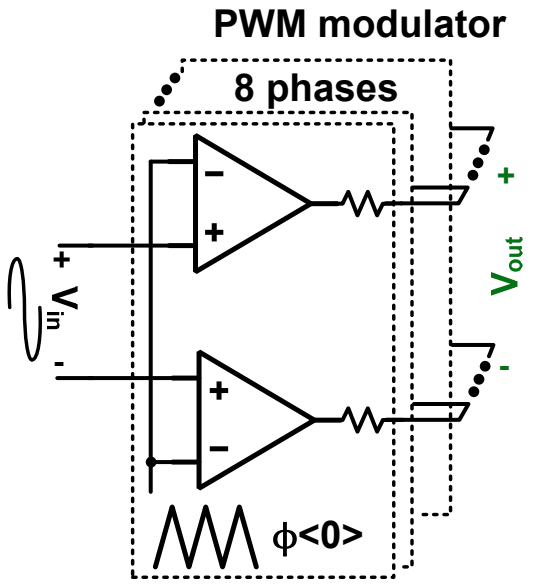
Stable SMOA bandwidth scales with technology

PWM Output Spectrum



PWM output spectrum for F_{PWM} = 300MHz

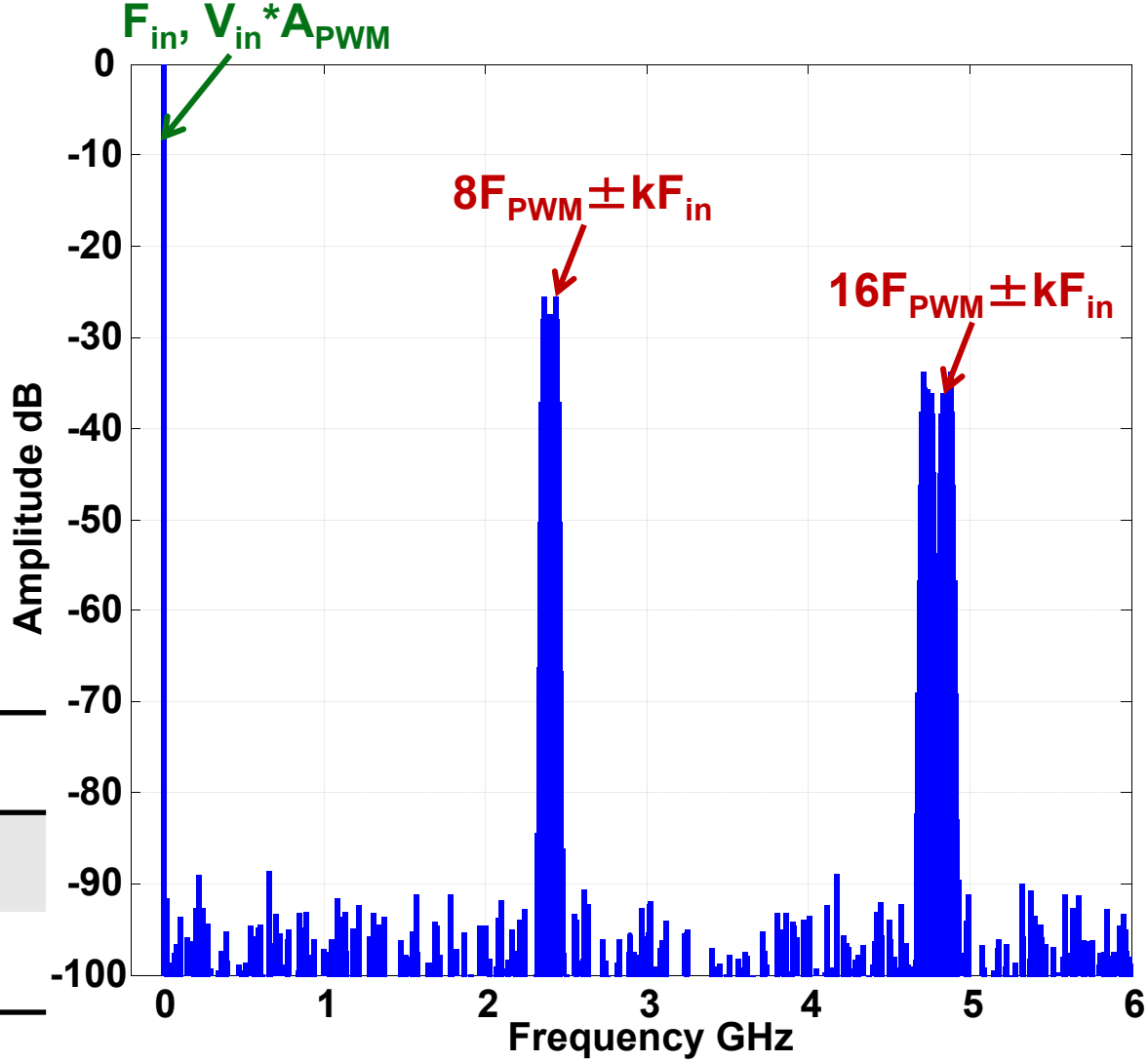
Multi-phase PWM Modulation



To push spurs to 2.4GHz

	F_{PWM}	V_{pp}	P_{diss}
8-ϕ	300MHz	91%	X
1-ϕ	2.4GHz	28%	8X

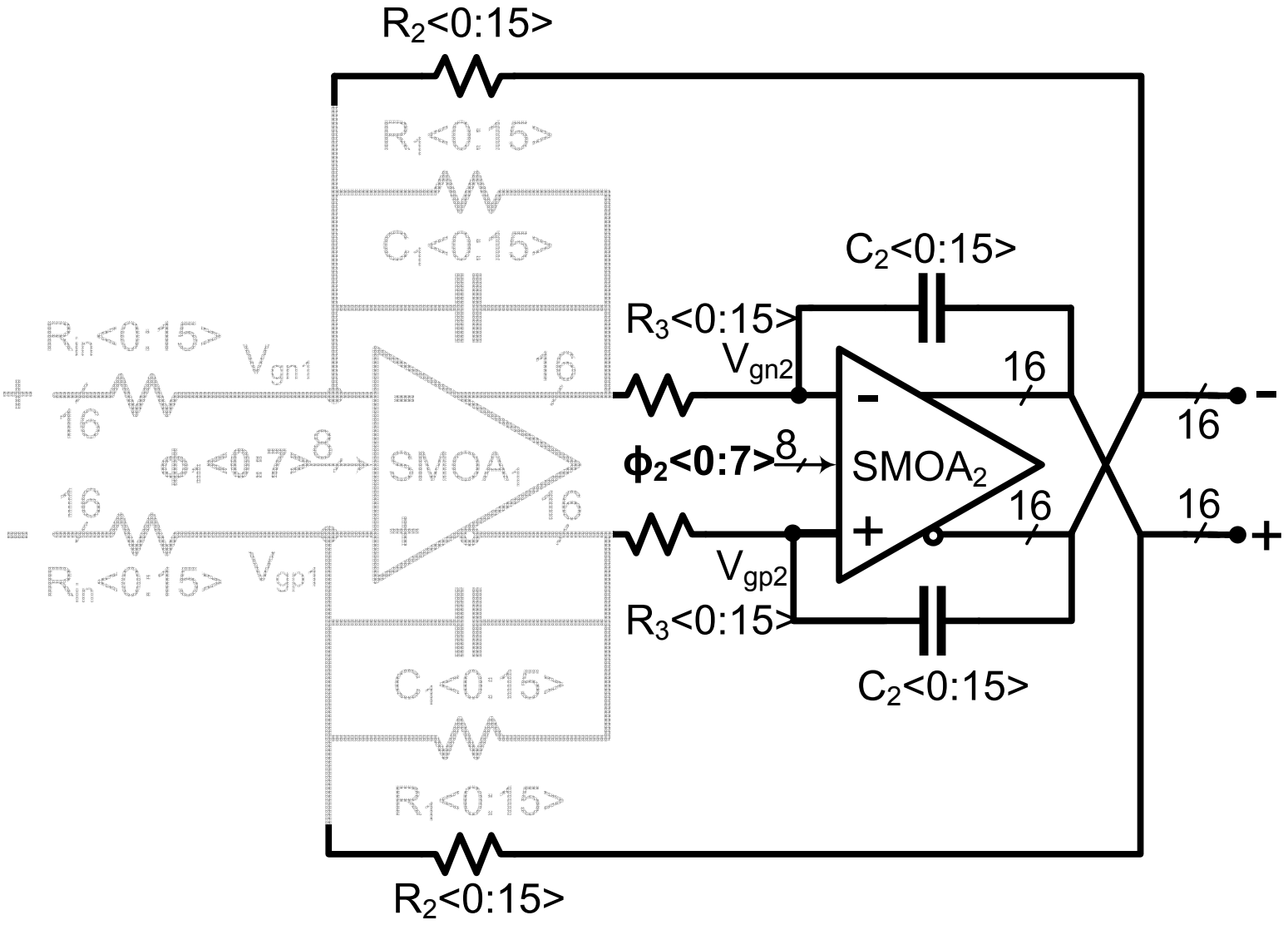
t_{min} = 150ps, V_{dd} = 0.6V



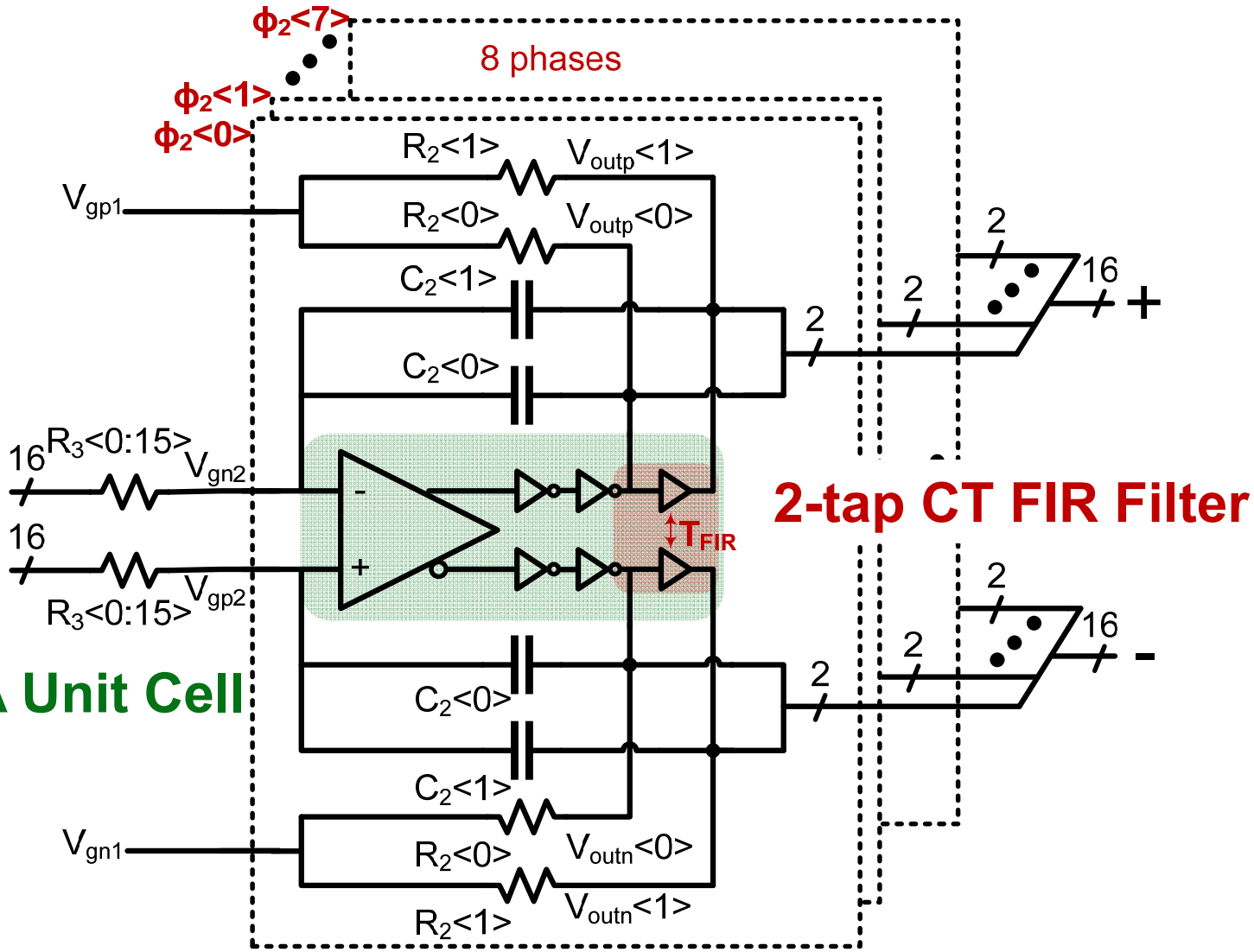
PWM output spectrum for N = 8 phases and F_{PWM} = 300MHz

Continuous-Time Filter Design using Proposed SMOAs

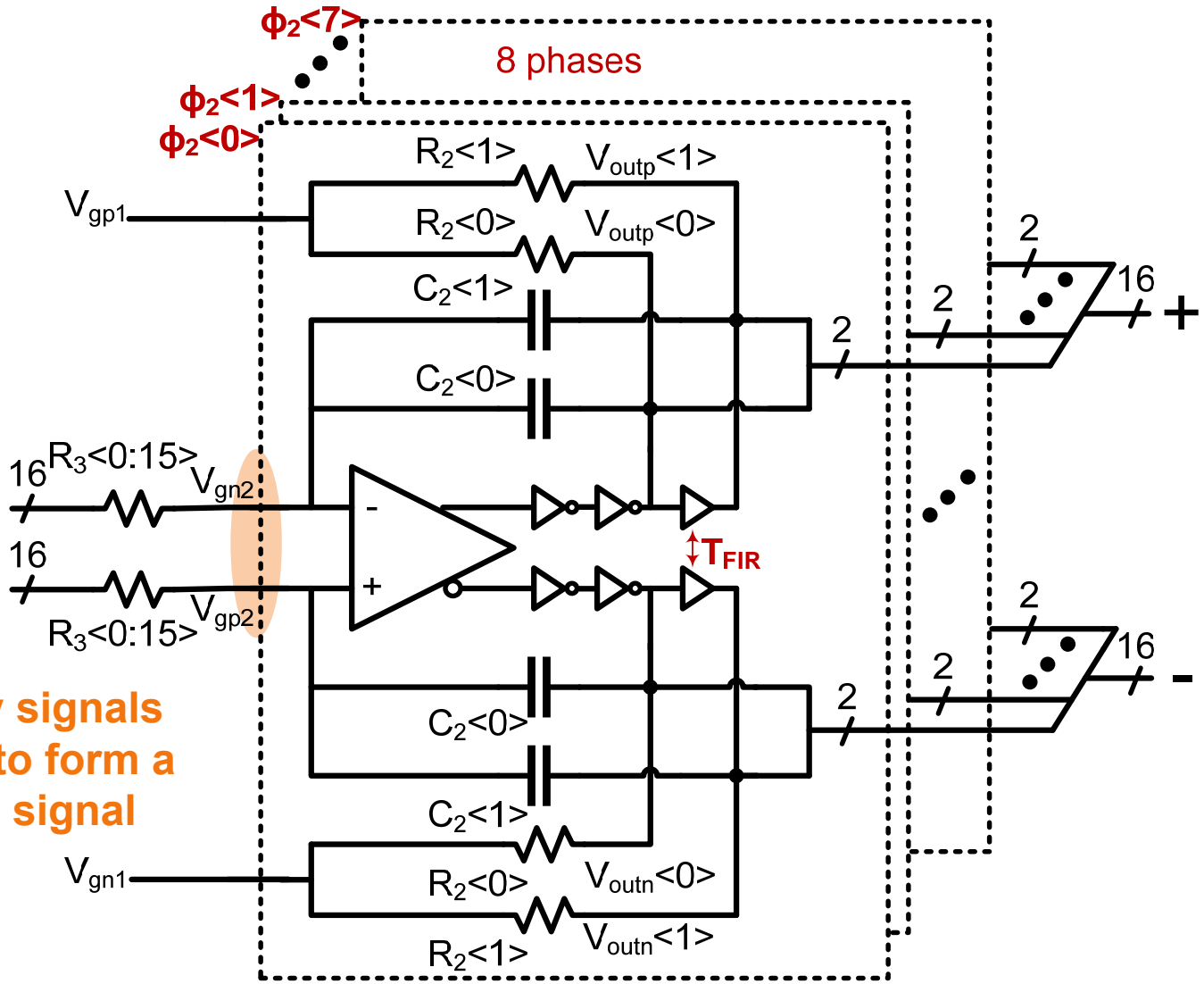
SMOA-RC Tow-Thomas biquad



8-phase SMOA Architecture

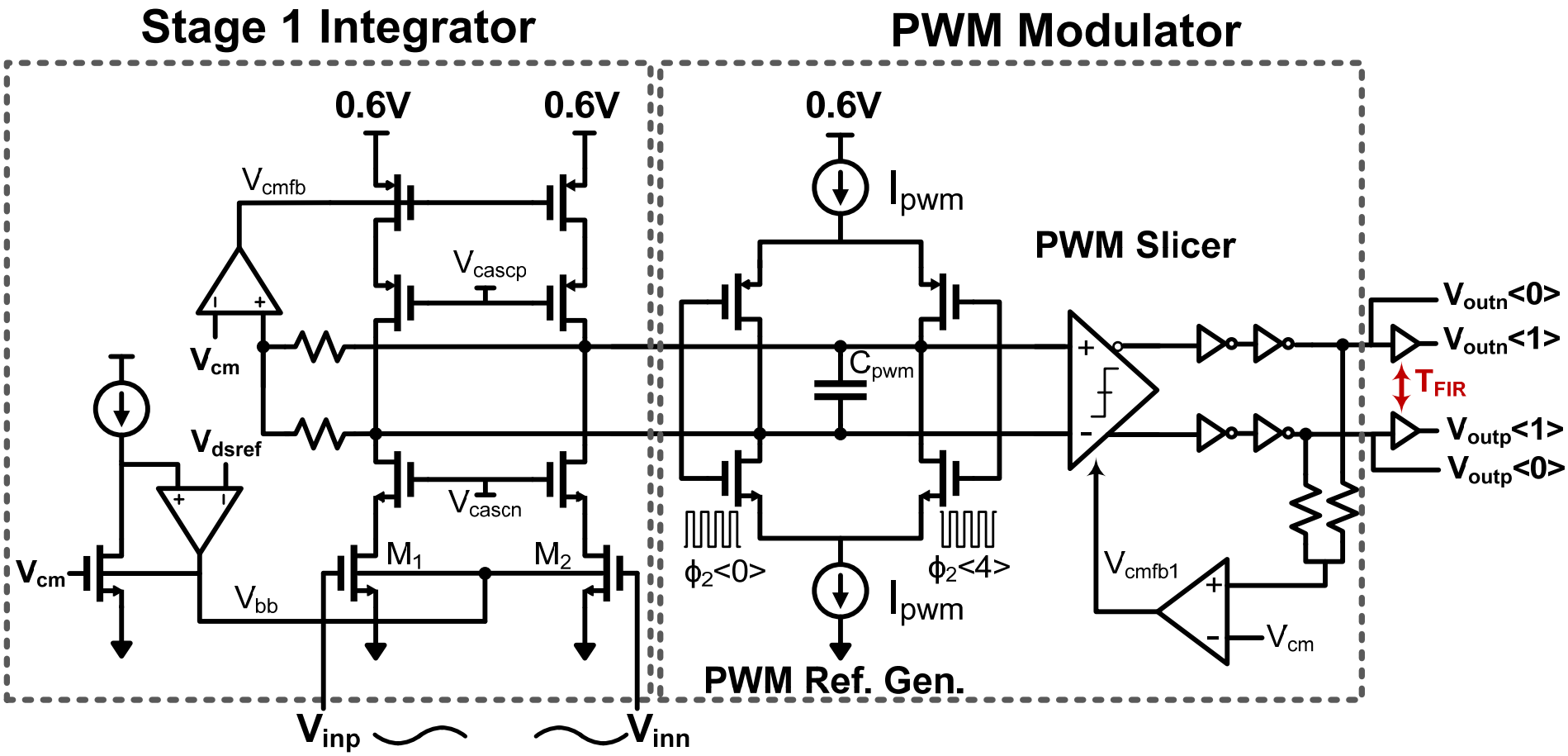


8-phase SMOA Architecture

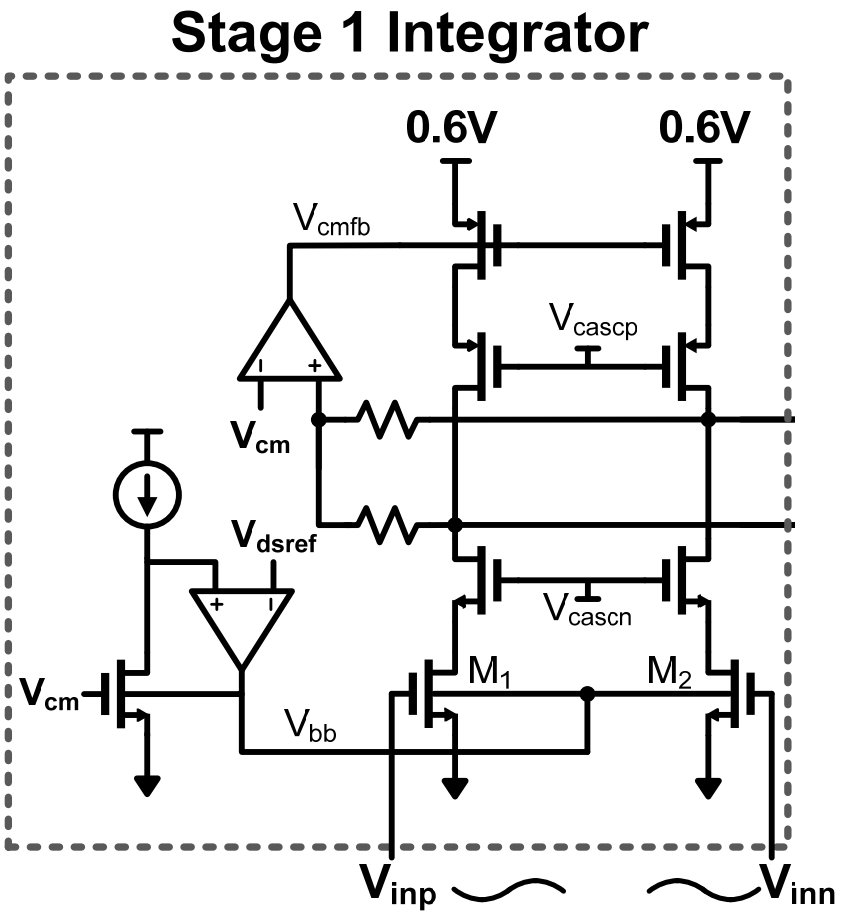


16 binary signals summed to form a 17-level signal

SMOA Unit Cell

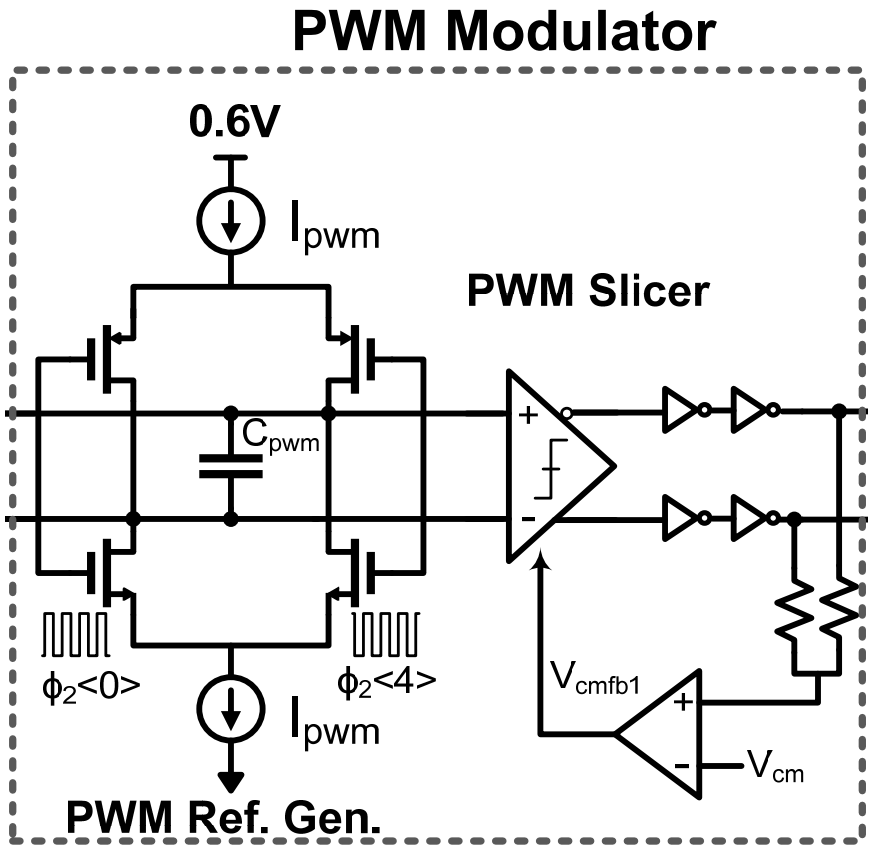


Stage 1 Integrator



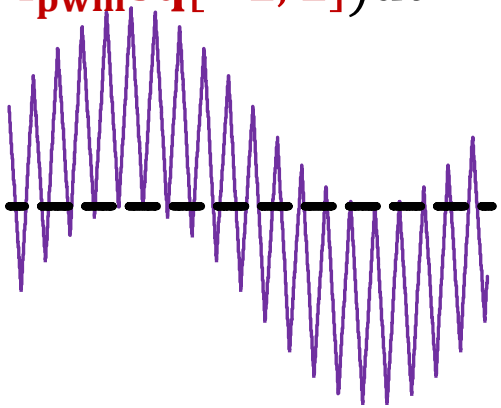
Pseudo-differential cascode amplifier with body-mirroring

PWM Modulator

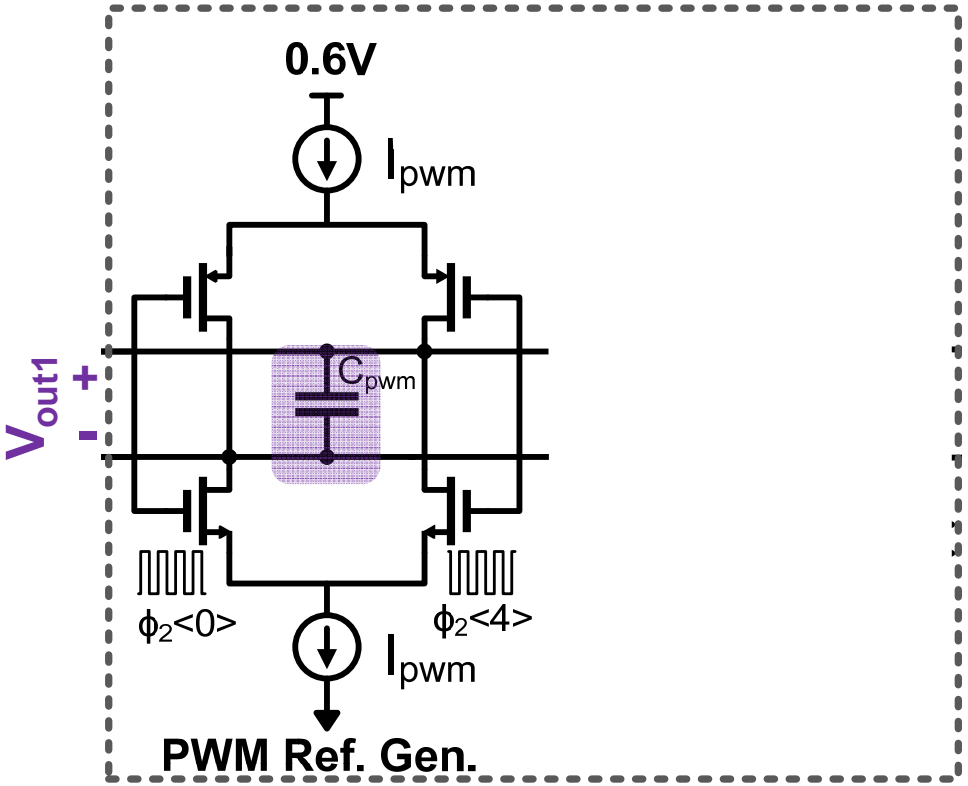


PWM Reference Ramp Generation

$$V_{out1}(t) = \frac{1}{C_{pwm}} \int \left(G_{m1s} V_{in}(t) - I_{pwm} sq[-1, 1] \right) dt$$

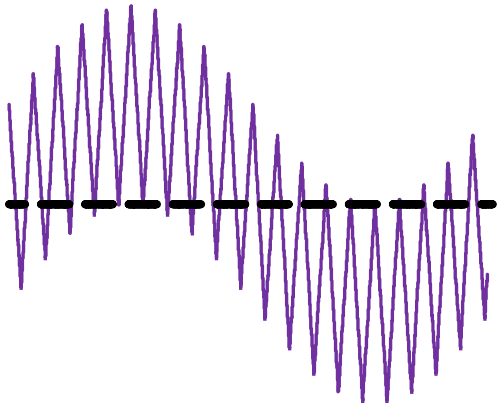


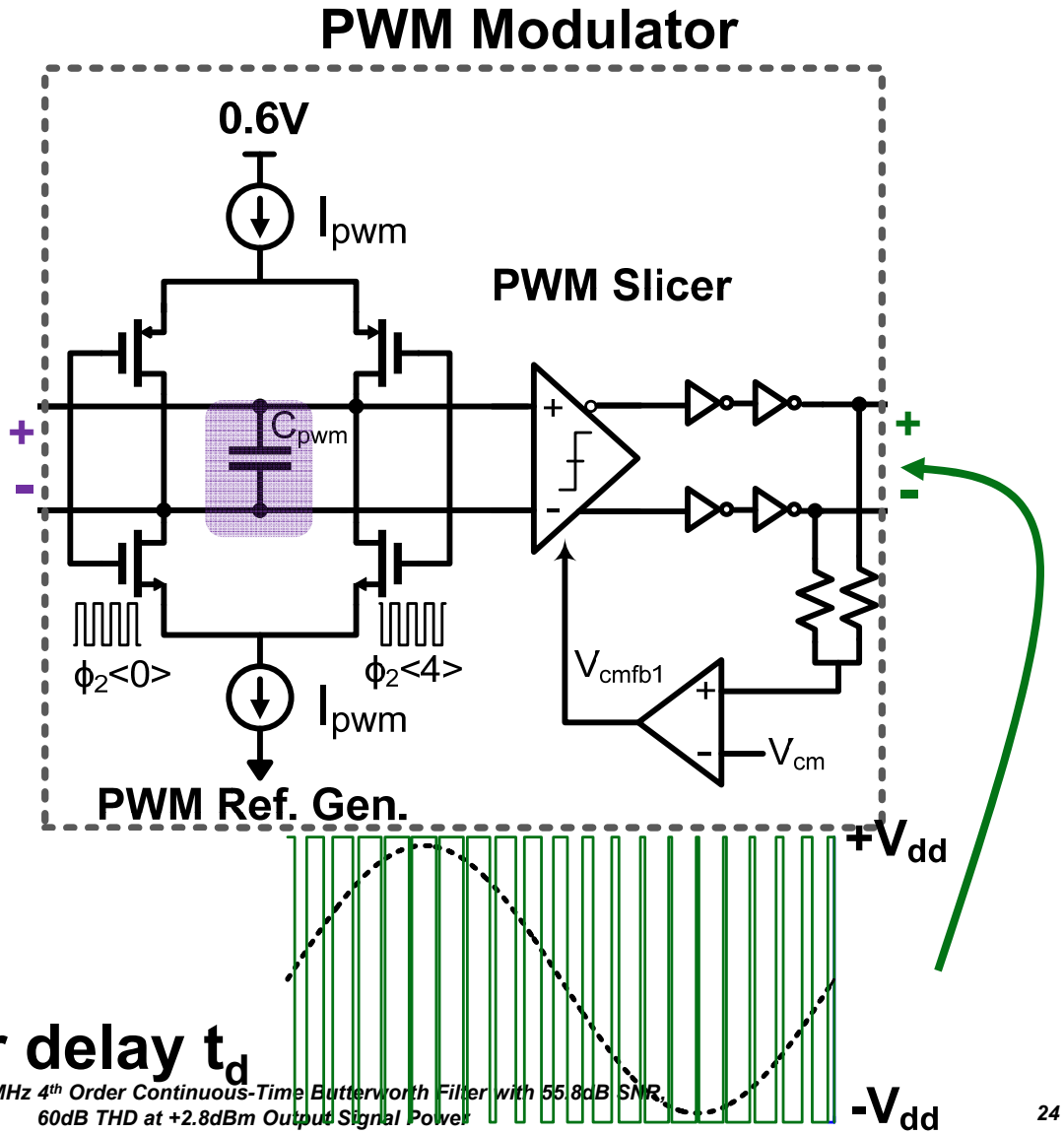
G_{m1s} – Trans-conductance of Stage I Integrator



Current domain subtraction of signal and reference

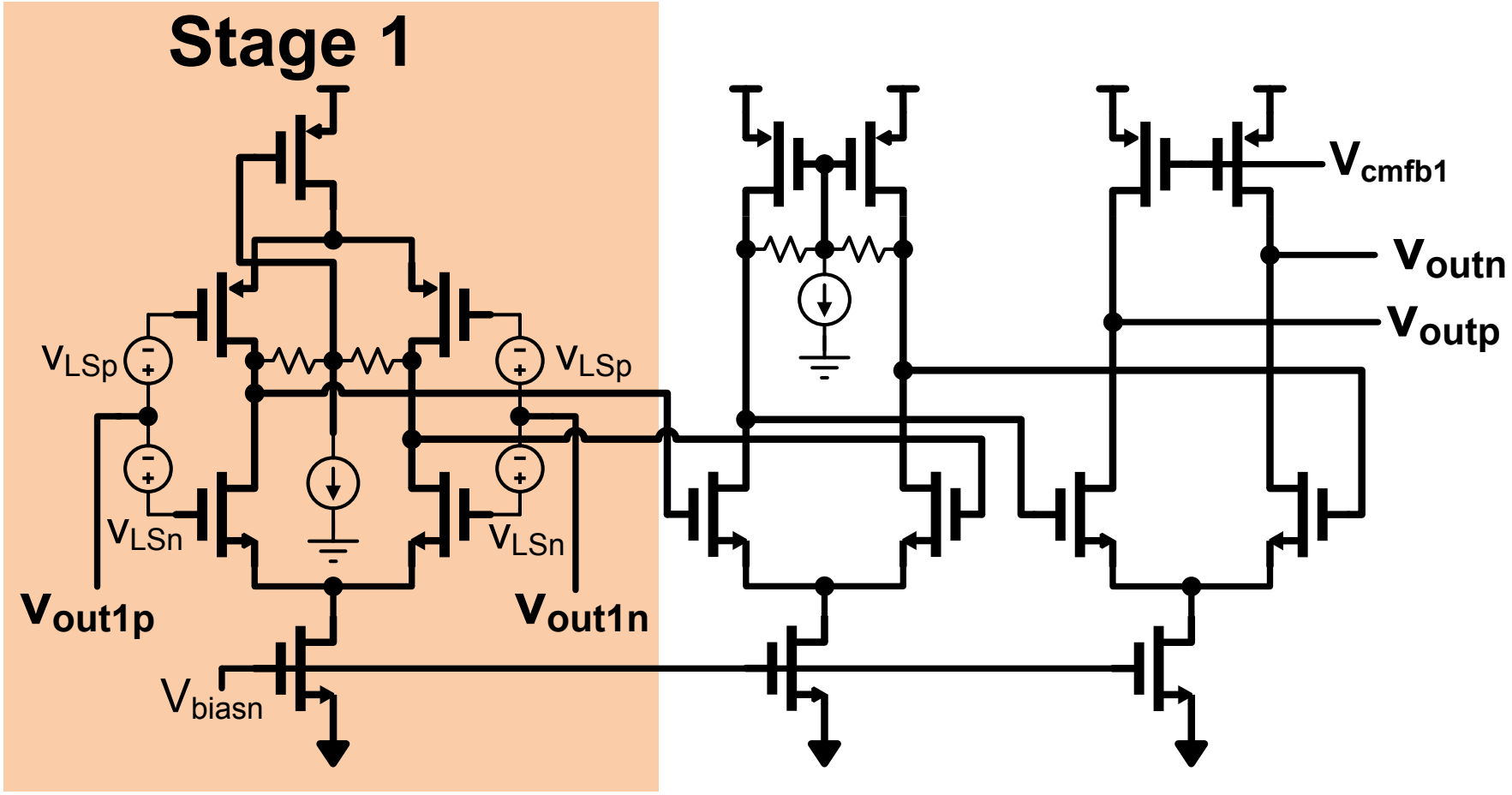
Continuous-time PWM Slicer





Minimize slicer delay t_d

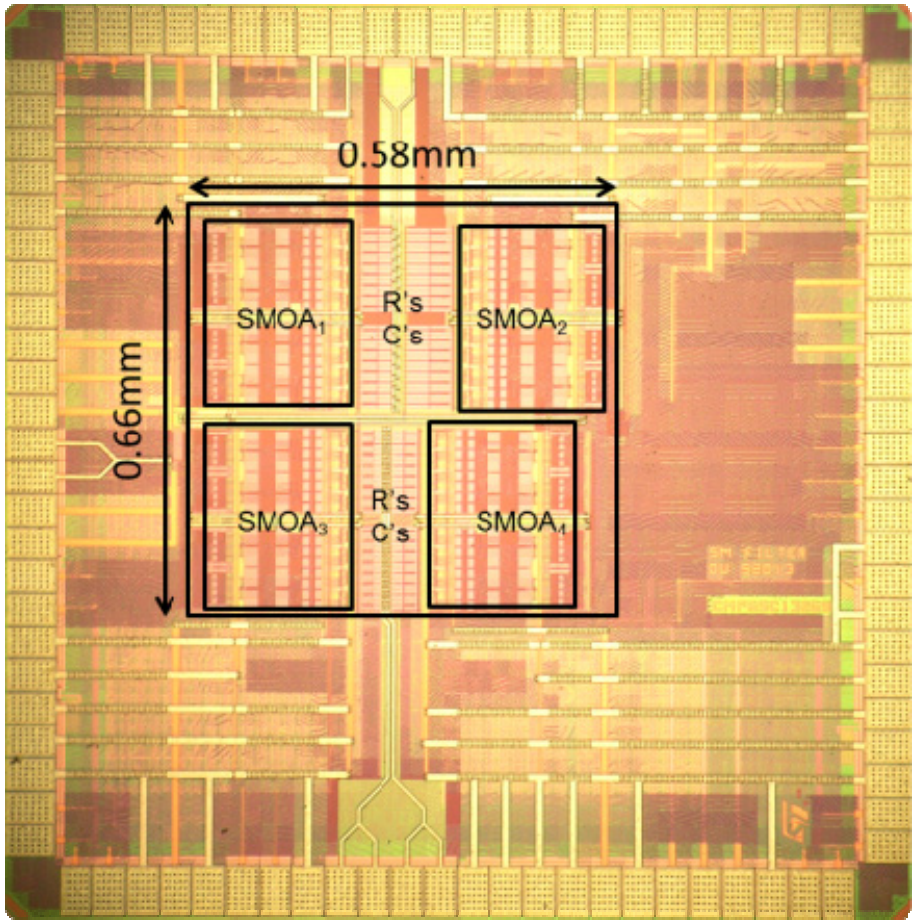
PWM Slicer



Cascade of differential amplifiers with partial current re-use

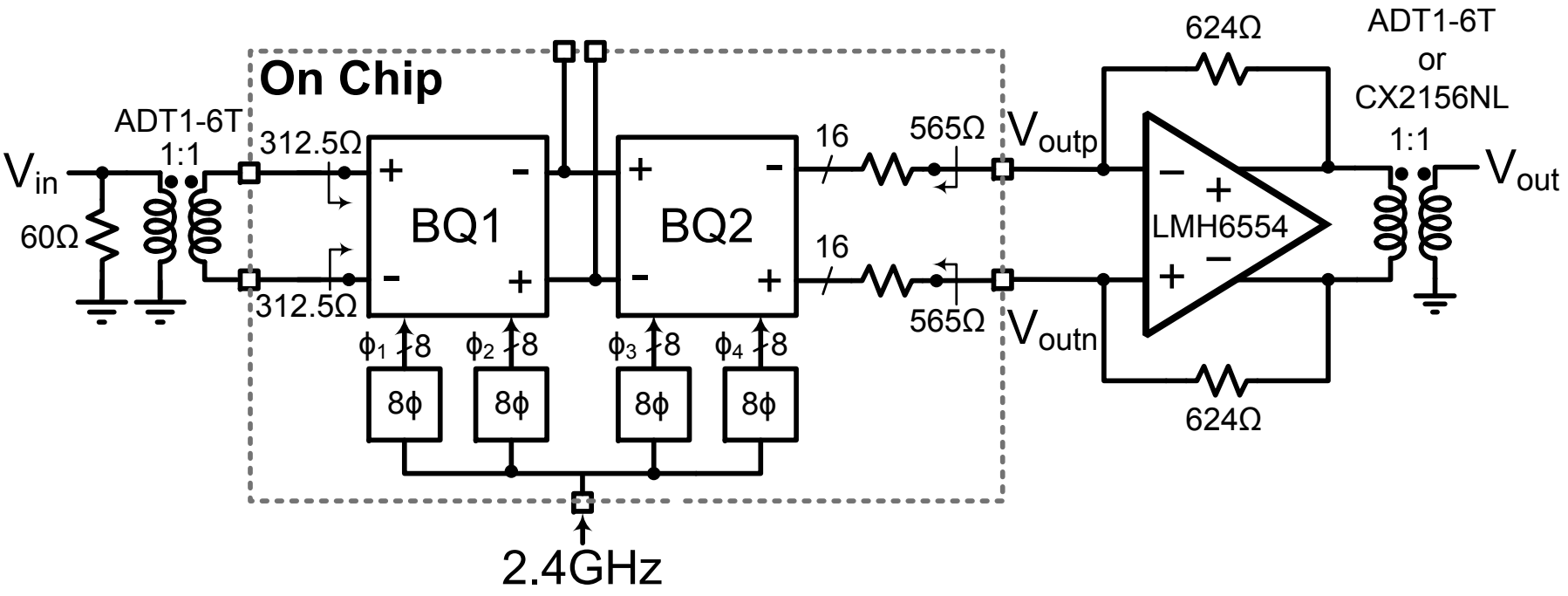
Prototype Filter Measurement Results

Die Photograph



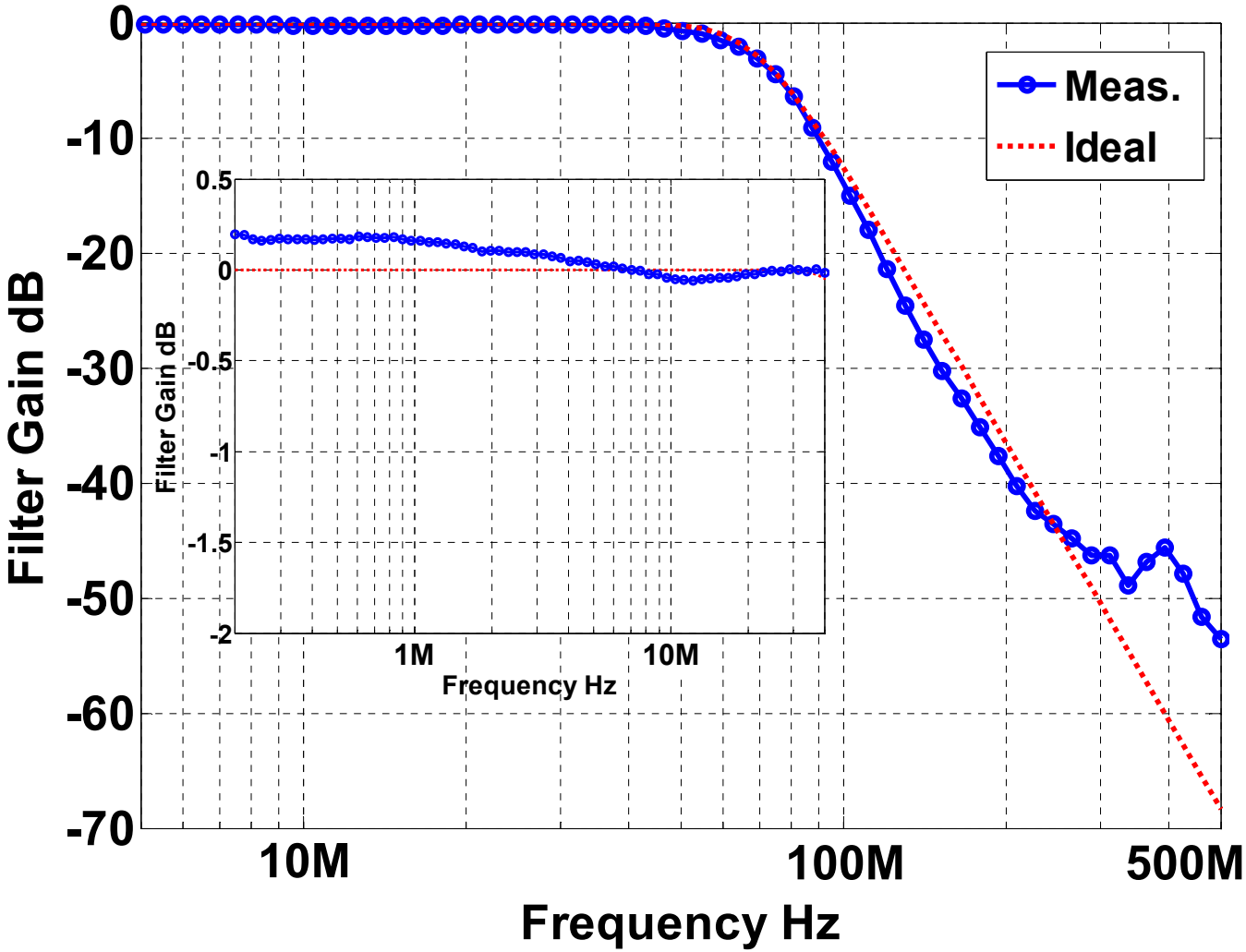
- Area = 0.38mm^2
- 65nm CMOS
- V_{dd} = 0.6V

Measurement Setup

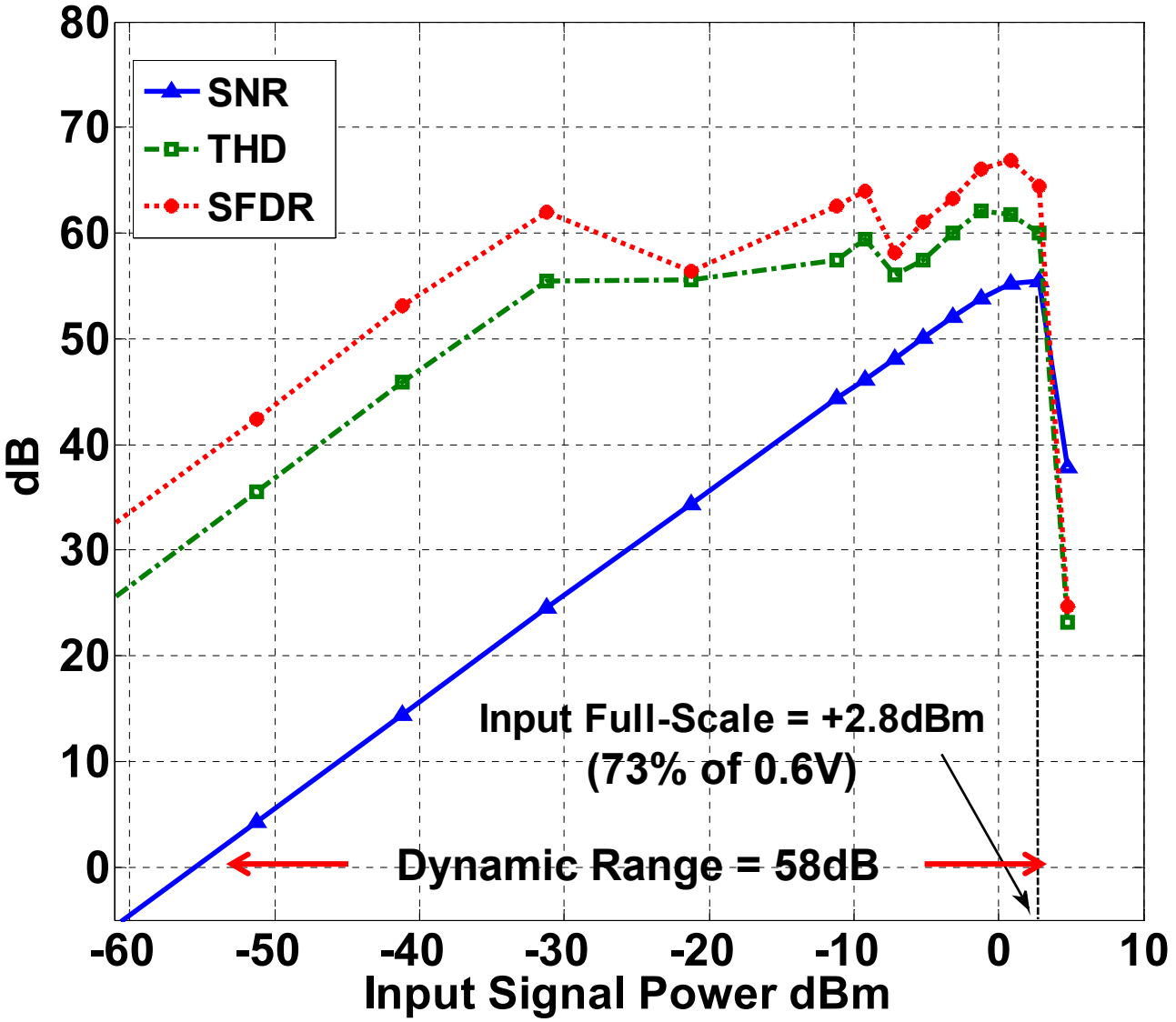


Output drives off-chip TIA *without any* signal attenuation

Frequency Response

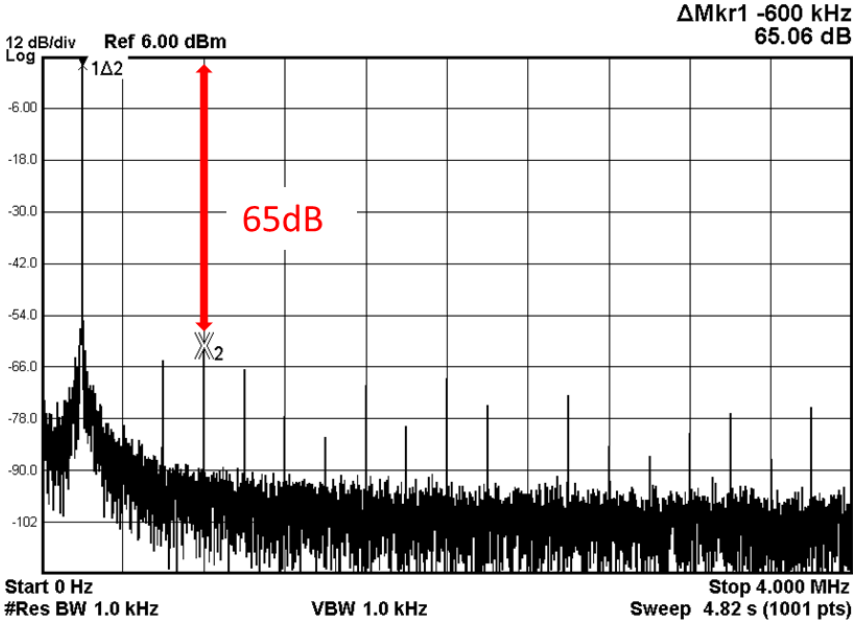


Input Amplitude Sweep

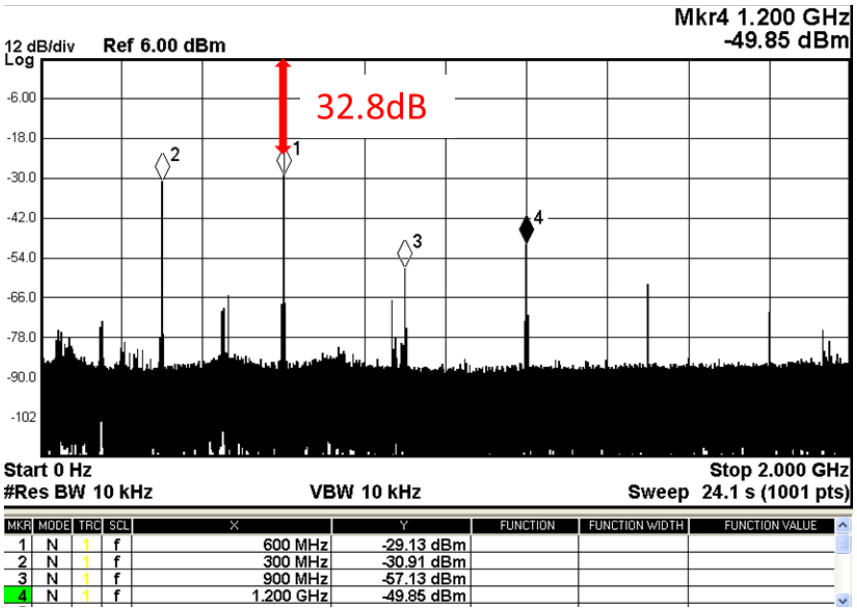


Spectrum for 200KHz +2.8dBm input

In-band output spectrum (0 – 4MHz)



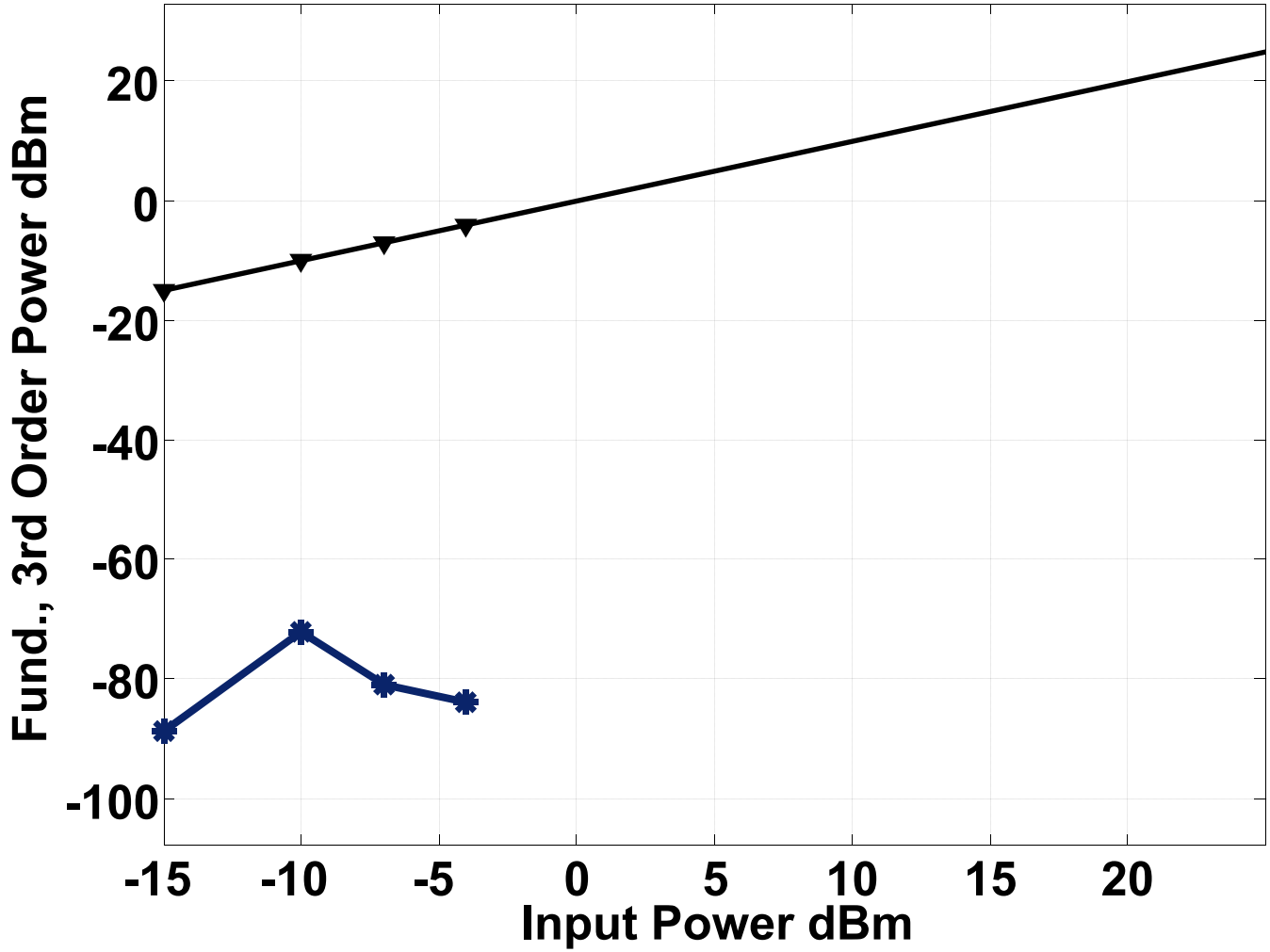
Complete output spectrum (0 – 2GHz)



SMOA phase mismatches cause residual spurs at 300MHz, 600MHz, etc.

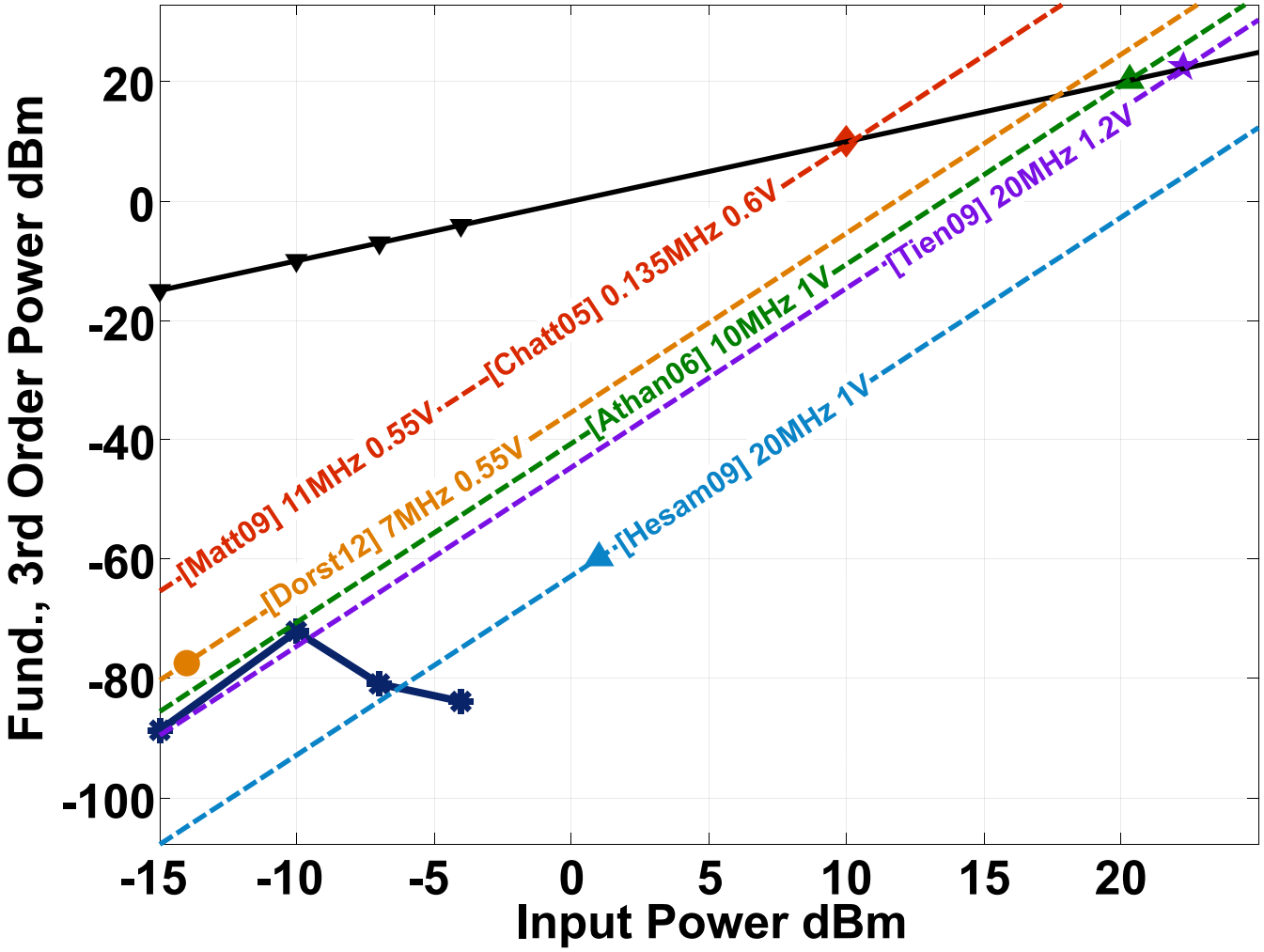
3rd Order Inter-Mod. Performance

In-band IM3 (1.95MHz and 2.05MHz)



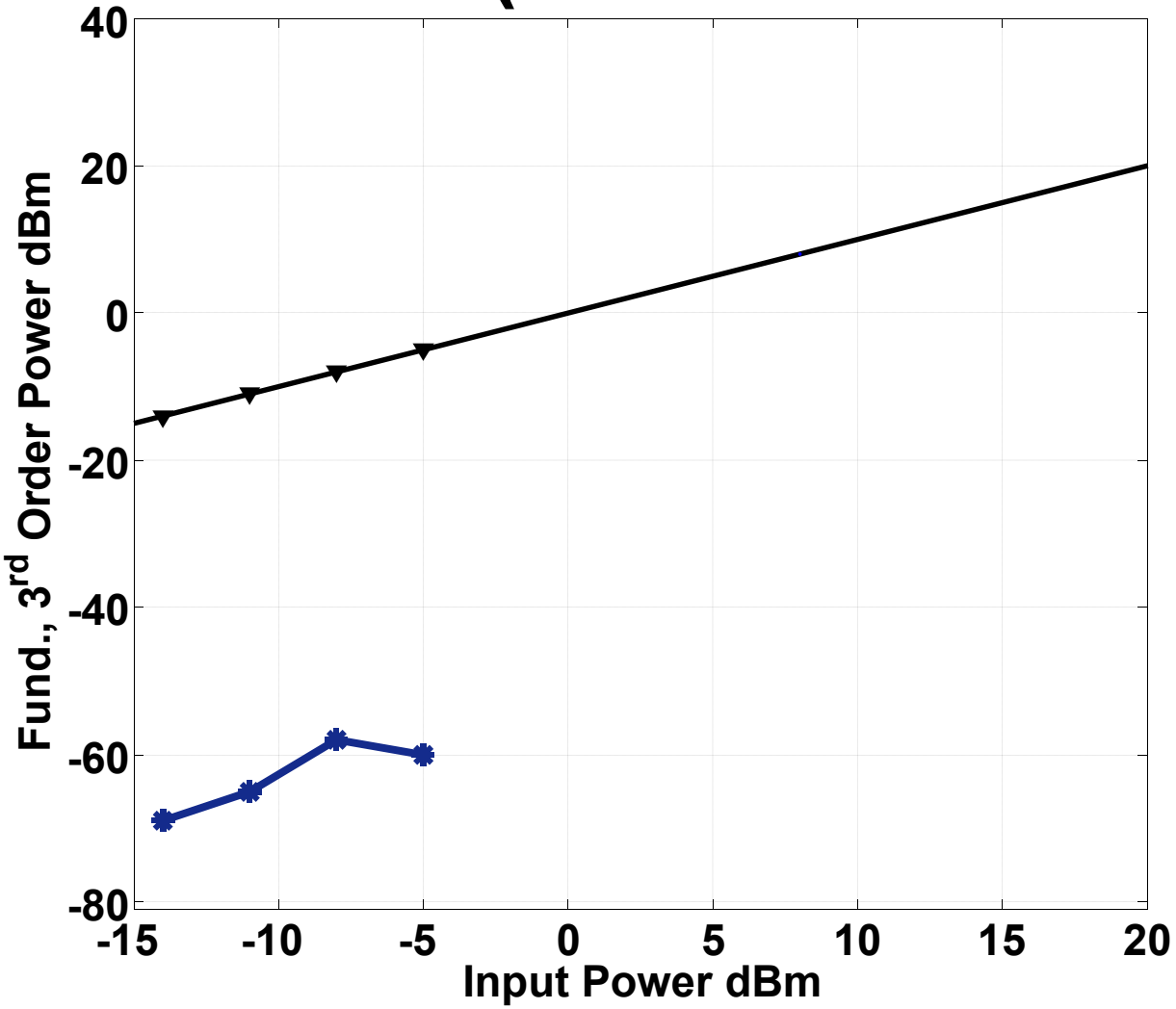
3rd Order Inter-Mod. Performance

In-band IM3 (1.95MHz and 2.05MHz)



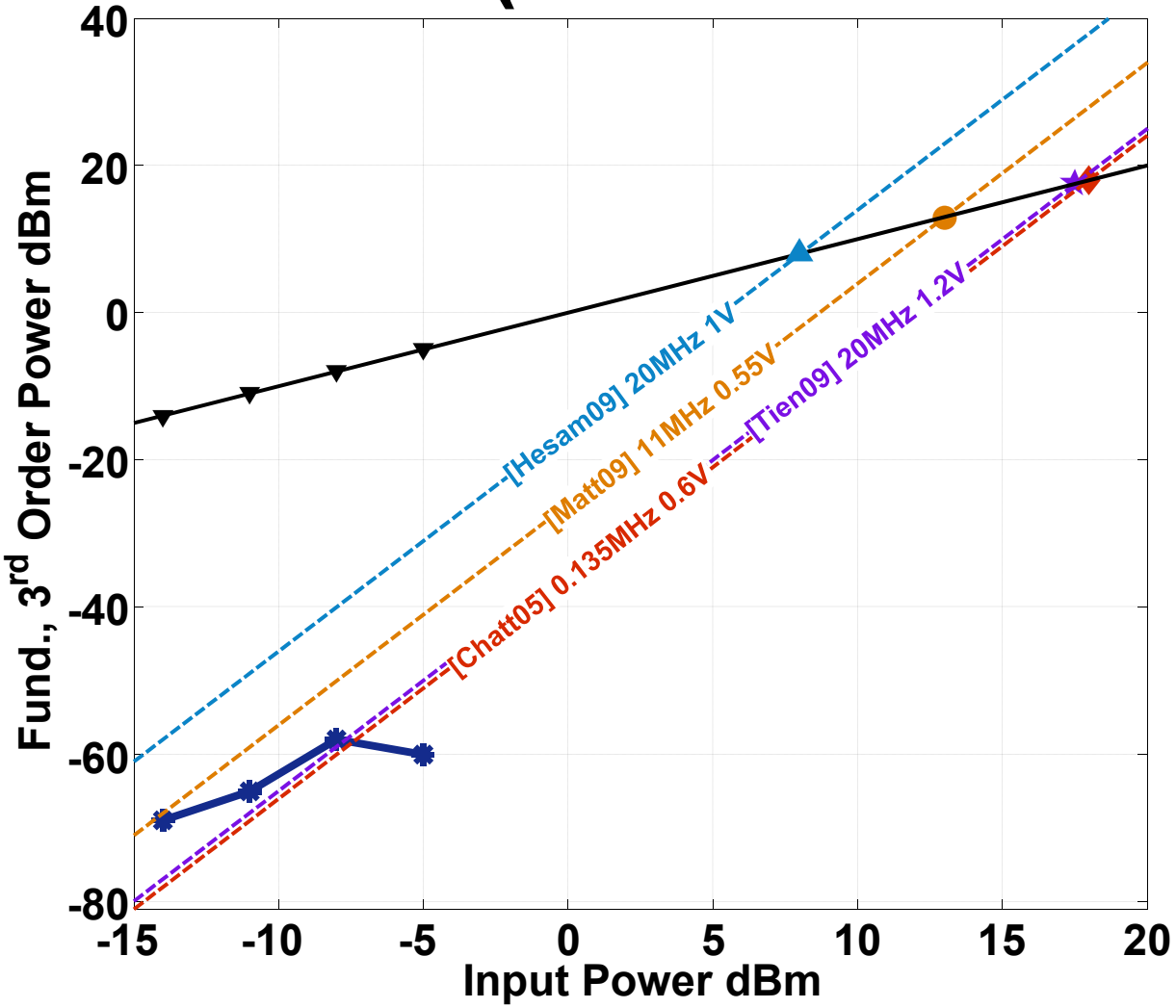
3rd Order Inter-Mod. Performance

Out-of-band IM3 (75.5MHz and 150MHz)

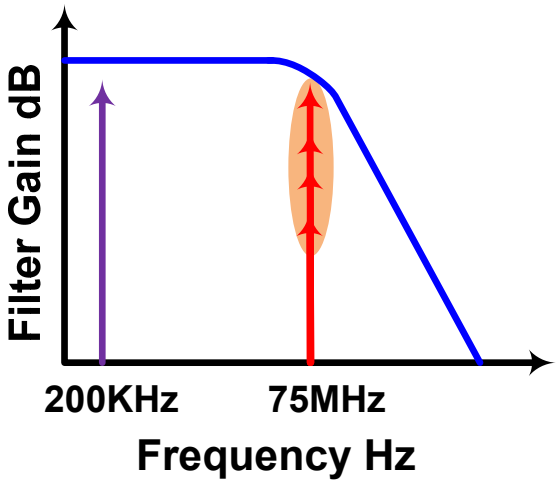


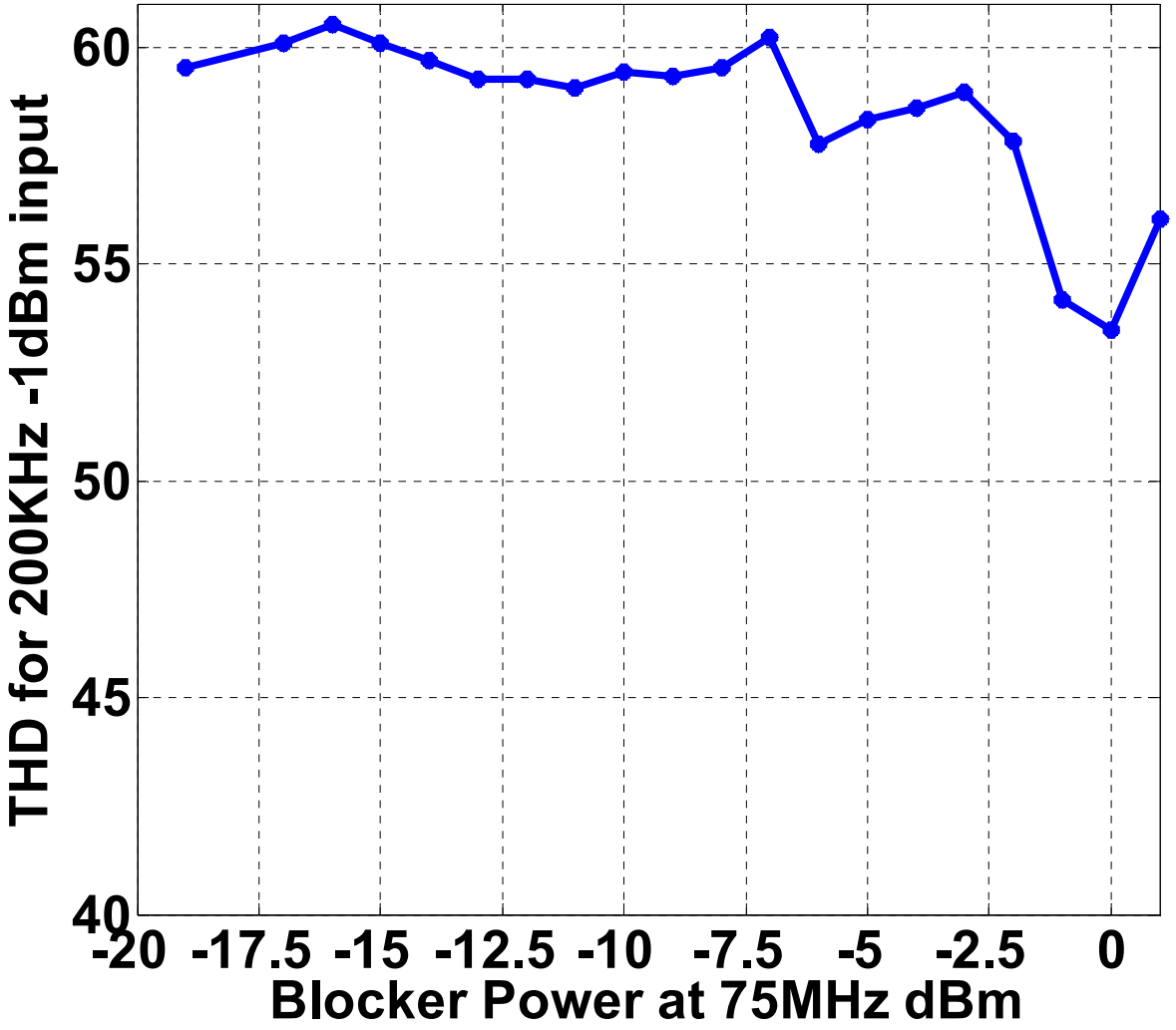
3rd Order Inter-Mod. Performance

Out-of-band IM3 (75.5MHz and 150MHz)



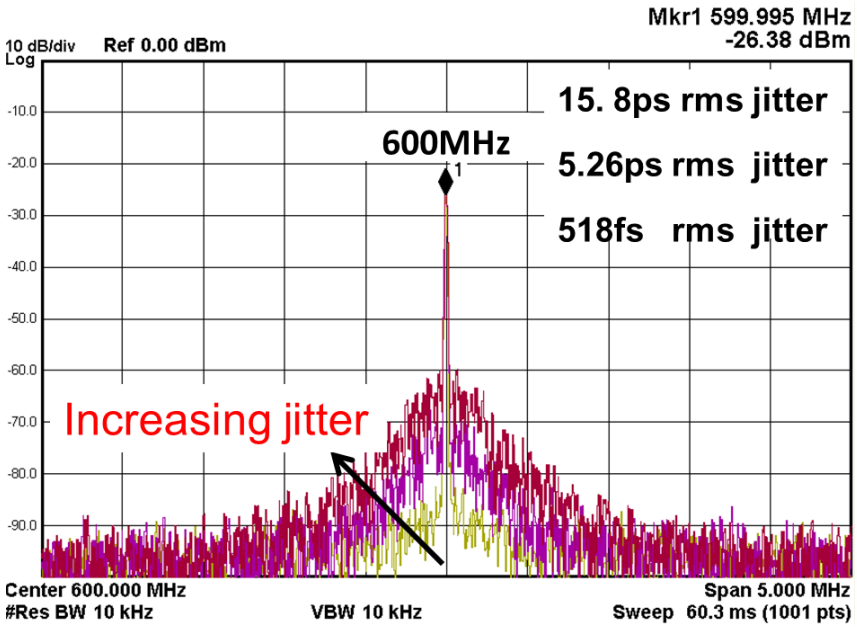
Linearity w/ Transition Band Blocker



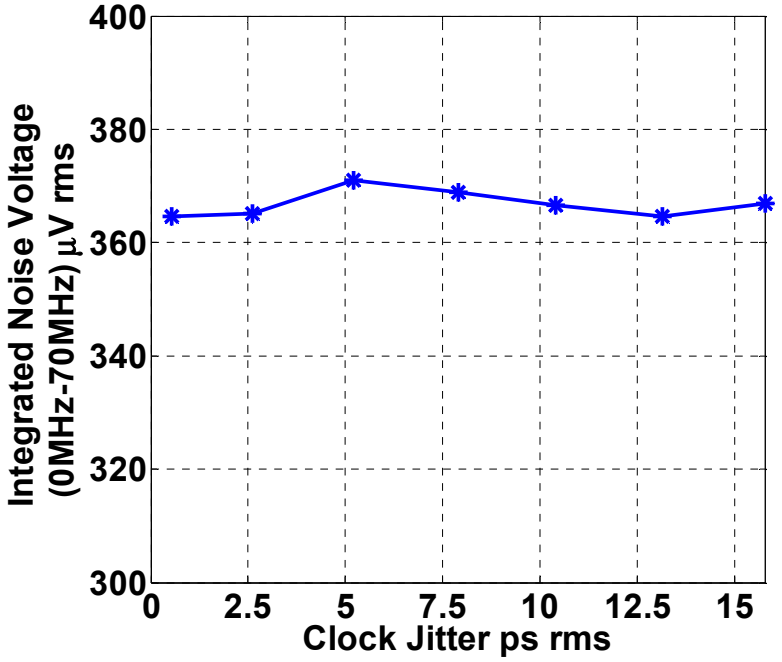


Effect of PWM Clock Jitter

Out-of-band effect of jitter at 600MHz modulation spur



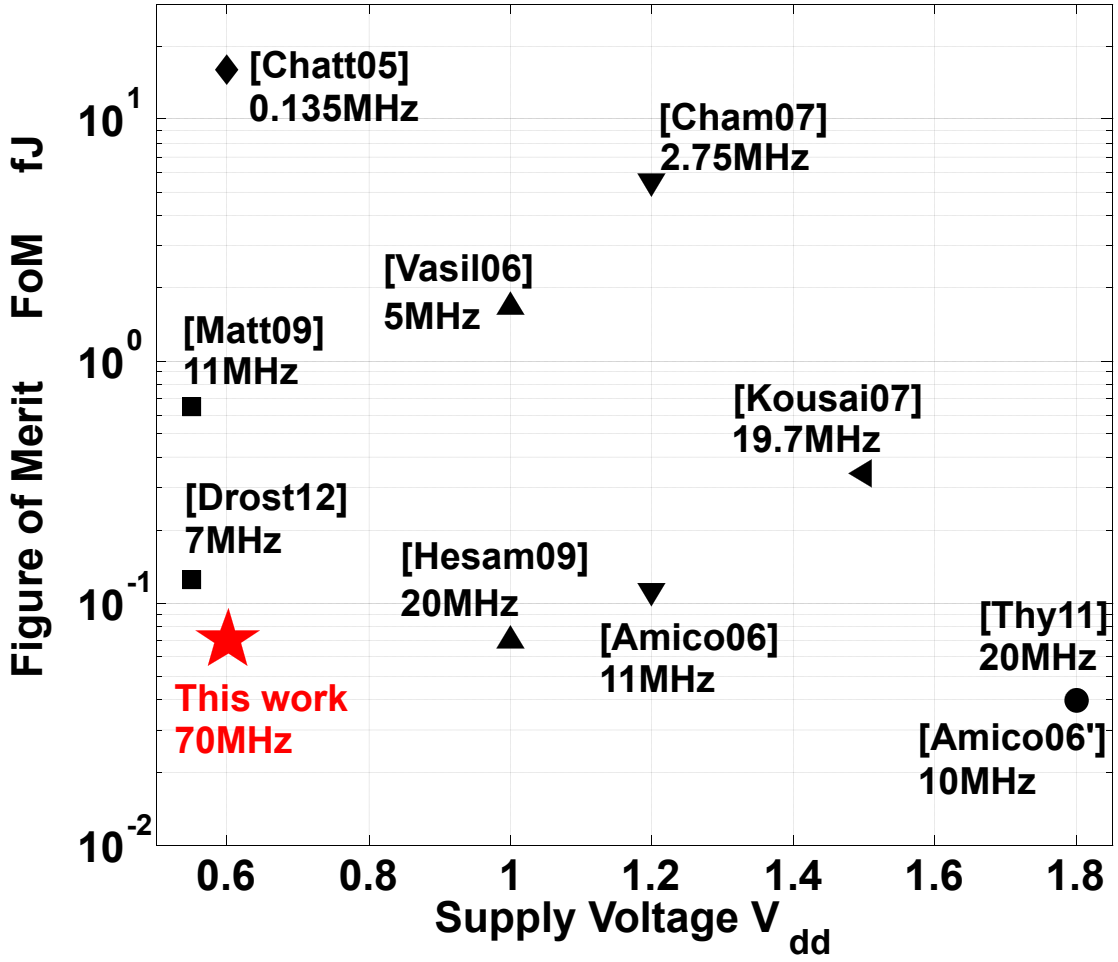
In-band integrated noise



Performance Summary

Technology		CMOS 65nm
Die Area		0.38mm^2
Supply		0.6V
Power	**Analog**	12.6mW
	Switched	12.8mW
	Clock Buf.	0.8mW
Bandwidth (f_{-3dB})		70MHz
Integ. Noise (0 to f_{-3dB})		365µV rms
Input Full-scale (FS)		+2.8dBm
Dynamic Range		58dB
SNR (@ FS)		55.8dB
THD (@ FS)		60dB
SFDR (@FS)		65dB

Comparison to State of the Art



$$\mathbf{FoM[Thy11]} = \frac{\mathbf{P}}{\mathbf{f_{-3dB}} \times \mathbf{N} \times \mathbf{SFDR}}$$

Conclusions

- Switched-mode operational amplifiers
  - Rail-to-rail signal swing at low V_{dd}
  - Load-agnostic amplifier bandwidth
  - Performance scales with technology

- 4^{th} order SMOA-RC Butterworth filter
  - Leverages faster devices and passives in feedback for excellent linearity performance
  - Blocker tolerance
  - Excellent FOM

Acknowledgments

- Didier Belot and STMicroelectronics for Silicon donation
- NSF Grant EECS 1309721 for partial funding
- Berkeley Design Automation for the Analog FastSpice Platform (AFS)
- Marianne Santangelo from Electrorent for test equipment

Thank You

References

- [Cham07] D. Chamla, “A Switchable-OrderGm-CBaseband Filter With Wide Digital Tuning for Configurable Radio Receivers,” IEEE JSSC Jul. 2007
- [Thy11] S. Thiyagarajan et. al, “Active-RC Filters Using the Gm-Assisted OTA-RC Technique,” IEEE JSSC, Jul. 2011.
- [Amico06] S. D’Amico, “A 4th-Order Active-G_m-RC Reconfigurable (UMTS/WLAN) Filter,” IEEE JSSC Jul. 2006.
- [Kousai07] S. Kousai, “A 19.7 MHz, Fifth-Order Active-RC Chebyshev LPF for Draft IEEE802.11n With Automatic Quality-Factor Tuning Scheme,” IEEE JSSC Nov. 2007.
- [Amico06'] S. D’Amico, “A 4.1-mW 10-MHz Fourth-Order Source-Follower-Based Continuous-Time Filter With 79-dB DR,” IEEE JSSC Dec. 2006
- [Drost12] B. Drost et. al., “Analog Filter Design Using Ring Oscillator Integrators,” IEEE JSSC Dec. 2012.
- [Matt09] M. De Matteis et. al., “A 0.55 V 60 dB-DR Fourth-Order Analog Baseband Filter,” IEEE JSSC Sept. 2009.

References

- [Chatt05] S. Chatterjee et. al., “A 0.5V Filter with PLL-Based Tuning in 0.18µm CMOS,” ISSCC 2005.
- [Hesam09] H. A. Aslanzadeh et. al., “A 1-V +31 dBm IIP3, Reconfigurable, Continuously Tunable, Power-Adjustable Active-RC LPF,” IEEE JSSC Feb. 2009
- [Vasil06] A. Vasilopoulos et. al., “A Low-Power Wideband Reconfigurable Integrated Active-RC Filter With 73 dB SFDR,” IEEE JSSC Sept. 2006.
- [Lo09] T. Y. Lo et. al., “A Wide Tuning Range G_m–C Filter for Multi-Mode CMOS Direct-Conversion Wireless Receivers,” IEEE JSSC Sept. 2009.

0.65V-Input-Voltage 0.6V-Output-Voltage 30ppm/°C Low-Dropout Regulator with Embedded Voltage Reference for Low-Power Biomedical Systems

Wei-Chung Chen, Yi-Ping Su, Yu-Huei Lee,

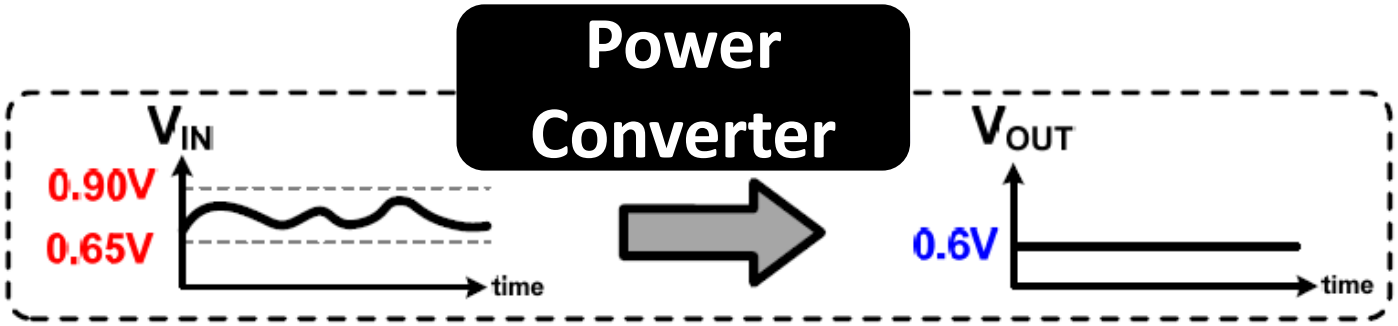
Chin-Long Wey, Ke-Horng Chen

National Chiao Tung University, Hsinchu, Taiwan

Outline

- Motivation
- Low-Dropout Regulator with Embedded Voltage Reference (LDO with EVR)
  - Circuit Implantation
  - Small-Signal Model
- Measurement Result
- Conclusion

Motivation



Output Voltage of Energy Harvester

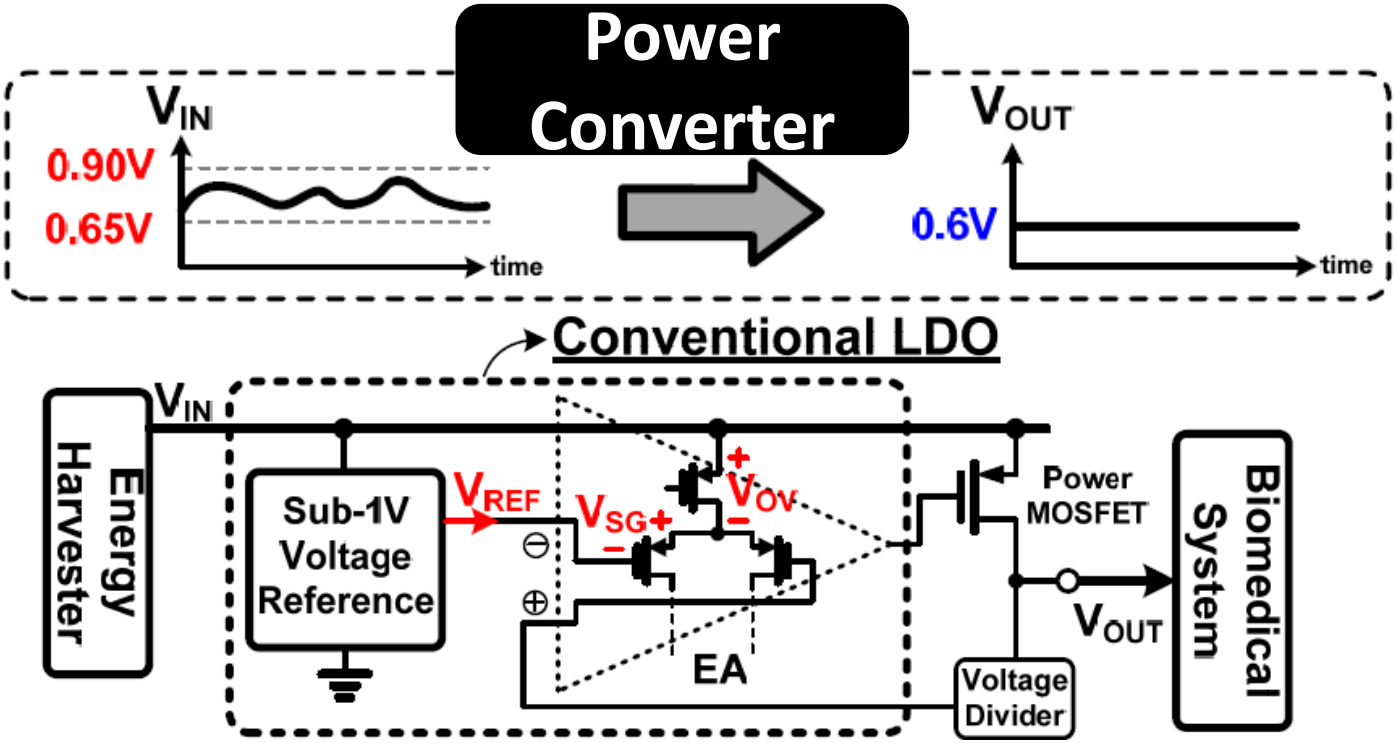
Supply Voltage of Biomedical System

- Design issues of Power Converter for Biomedical system
  - Compact Size
  - Low Cost

➔ No Inductor and Capacitor

➔ Low Dropout Regulator (LDO)

Motivation



Design Challenge

$$V_{IN} > |V_{tp}| + 2V_{OV} + V_{REF}$$

$$V_{IN} = 0.9V \sim 0.65V$$

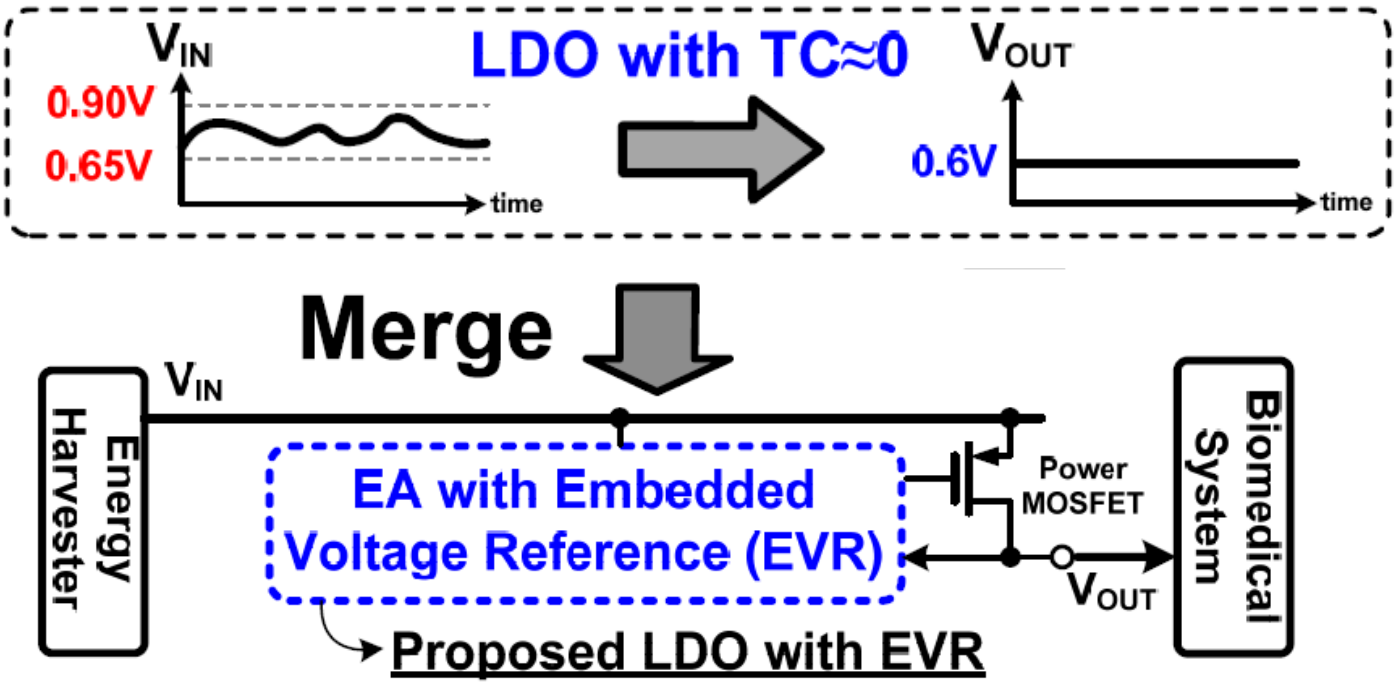
$$|V_{tp}| = 0.4 \sim 0.2V,\ V_{OV} = 0.1V$$

➔ $V_{REF} < 0.25V \sim 0.05V$

➔ **Hard to implement**

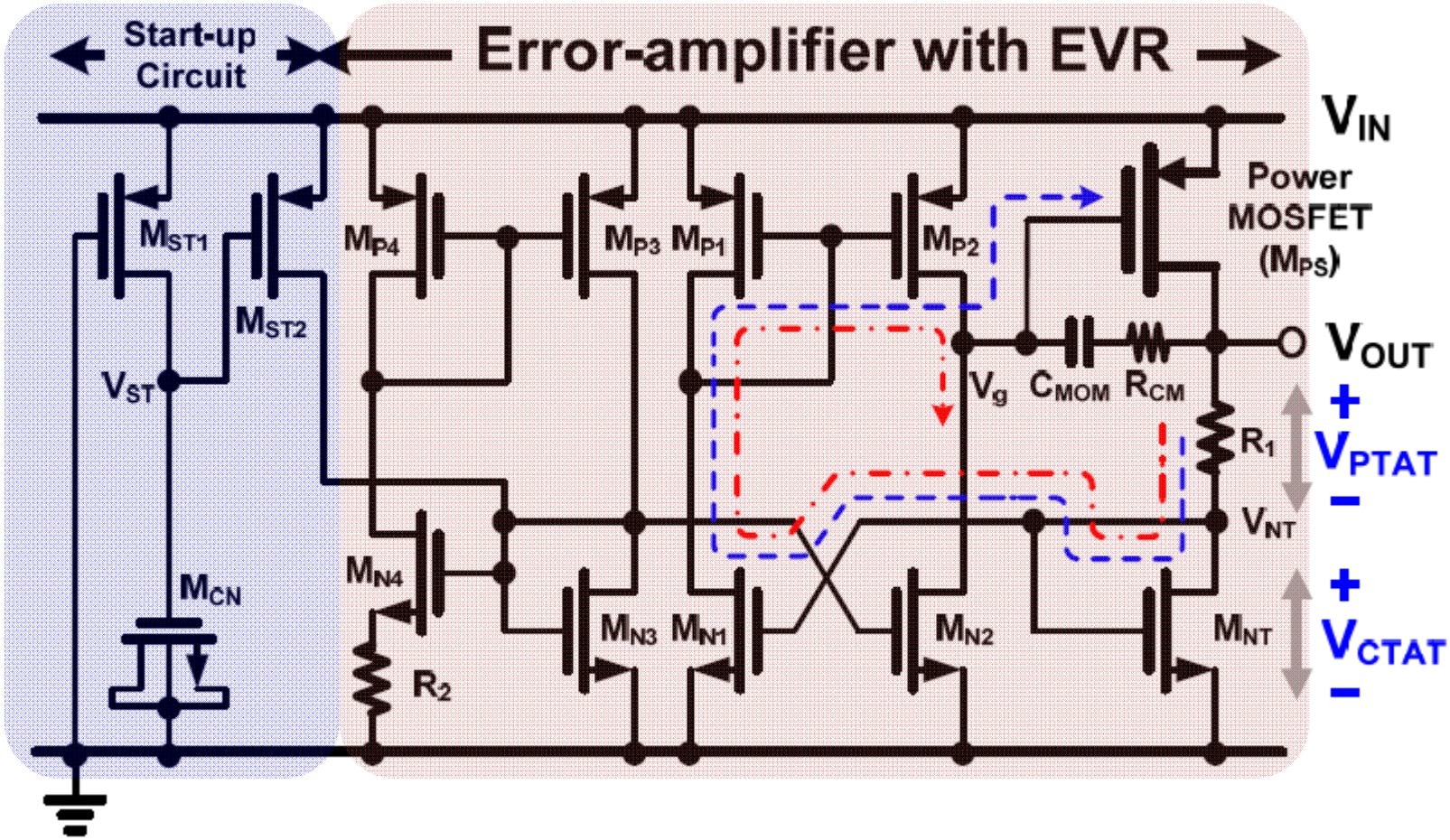
➔ **Temperature Coefficient (TC) is not zero**

Motivation

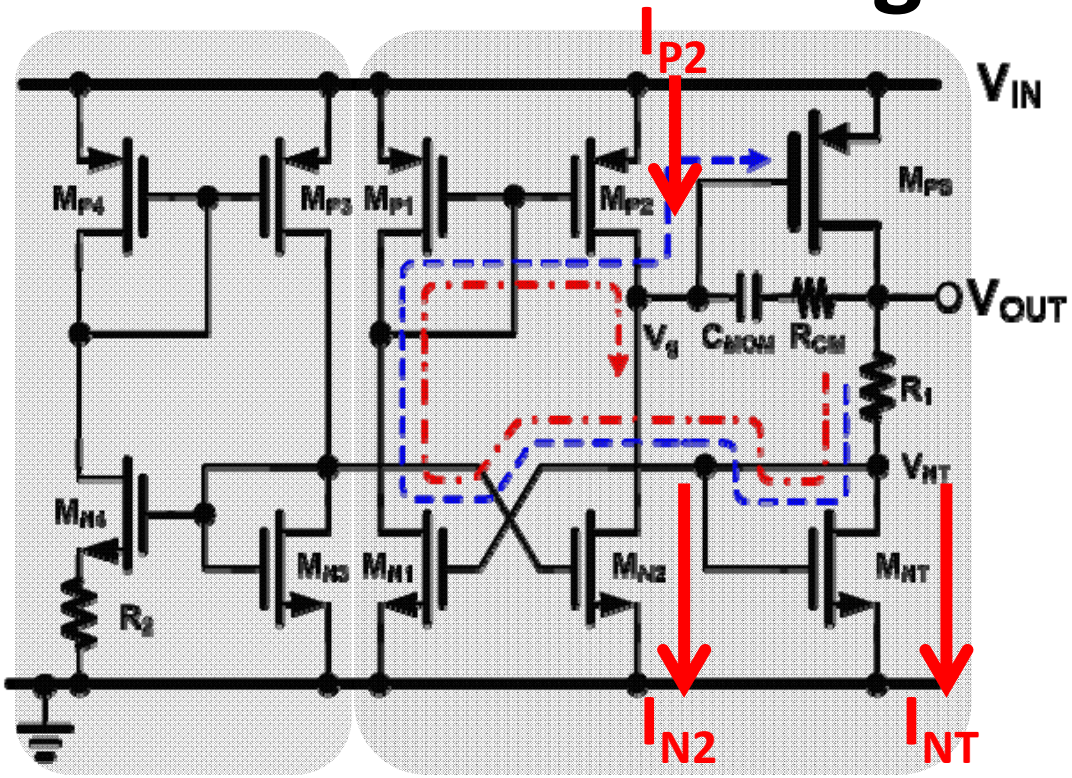


- **Without Complex Structure**
- **Driving Capability**
- **Low Temperature Coefficient (TC)**

Low-Dropout Regulator with Embedded Voltage Reference (EVR)



Low-Dropout Regulator with Embedded Voltage Reference (EVR)



Reference Current

(sub-threshold region)

$$I_{N2} = V_T \ln\left(\frac{S_{MN4} S_{MP3}}{S_{MN3} S_{MP4}}\right) / R_2$$

Current-mirror Path

$$K \cdot I_{P2} = I_{NT}$$

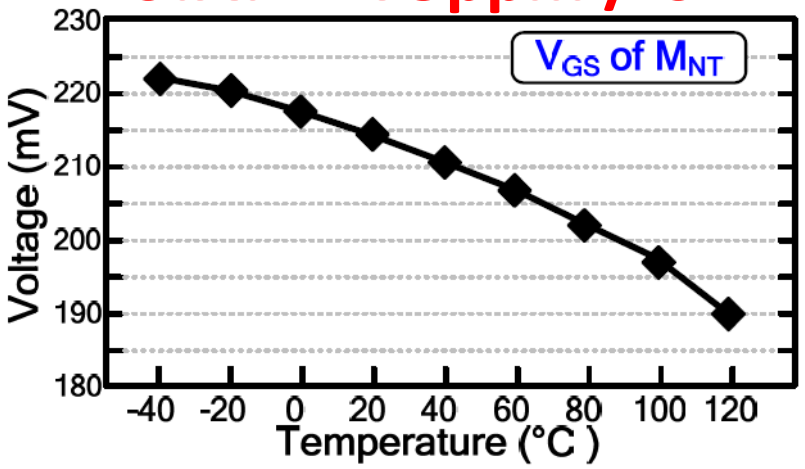
Feedback Path

$$I_{N2} = I_{P2} \cdot [A_C / (1 + A_C)]$$

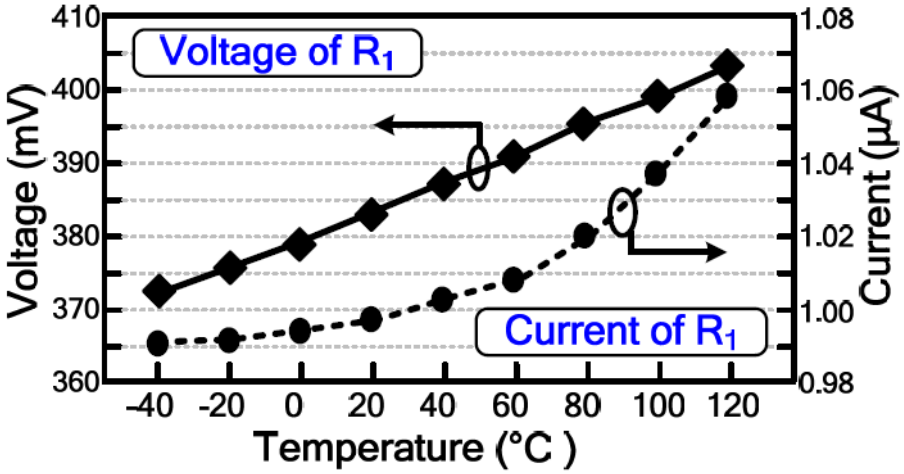
$$V_{OUT} = \underbrace{V_{GS\_MNT}}_{\text{CTAT}} + \underbrace{K \cdot V_T}_{\text{PTAT}} \ln\left(\frac{S_{MN4} S_{MP3}}{S_{MN3} S_{MP4}}\right) \underbrace{\frac{R_1}{R_2}}_{\text{Const.}}$$

Output Voltage Versus Temperature

CTAT=-175ppm /°C



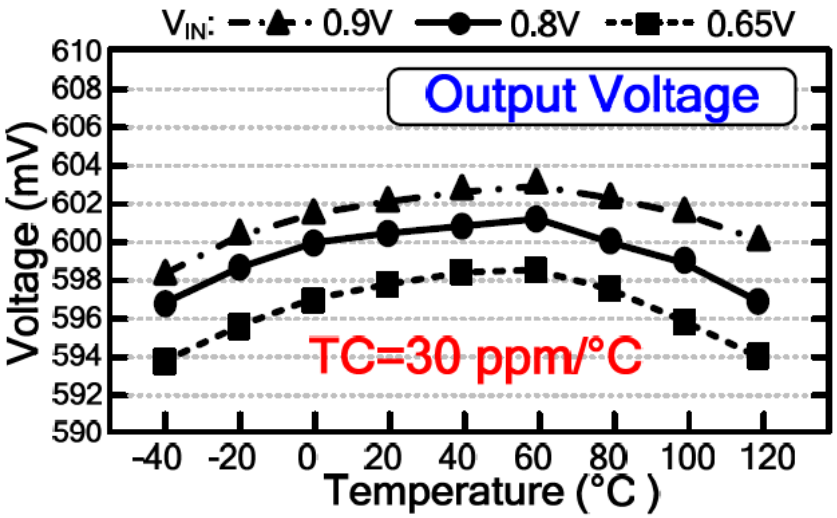
PTAT



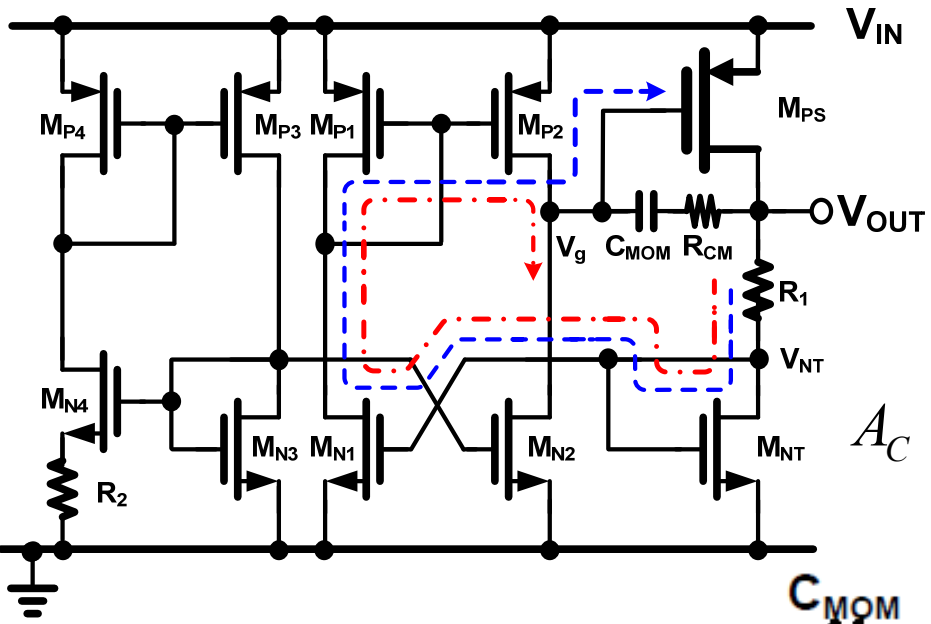
$$V_{OUT} = V_{GS\_MNT} + K \cdot V_T \ln\left(\frac{S_{MN4}S_{MP3}}{S_{MN3}S_{MP4}}\right)\frac{R_1}{R_2}$$

CTAT **PTAT** **Const.**

$$\frac{\partial V_{OUT}}{\partial T} = 0$$

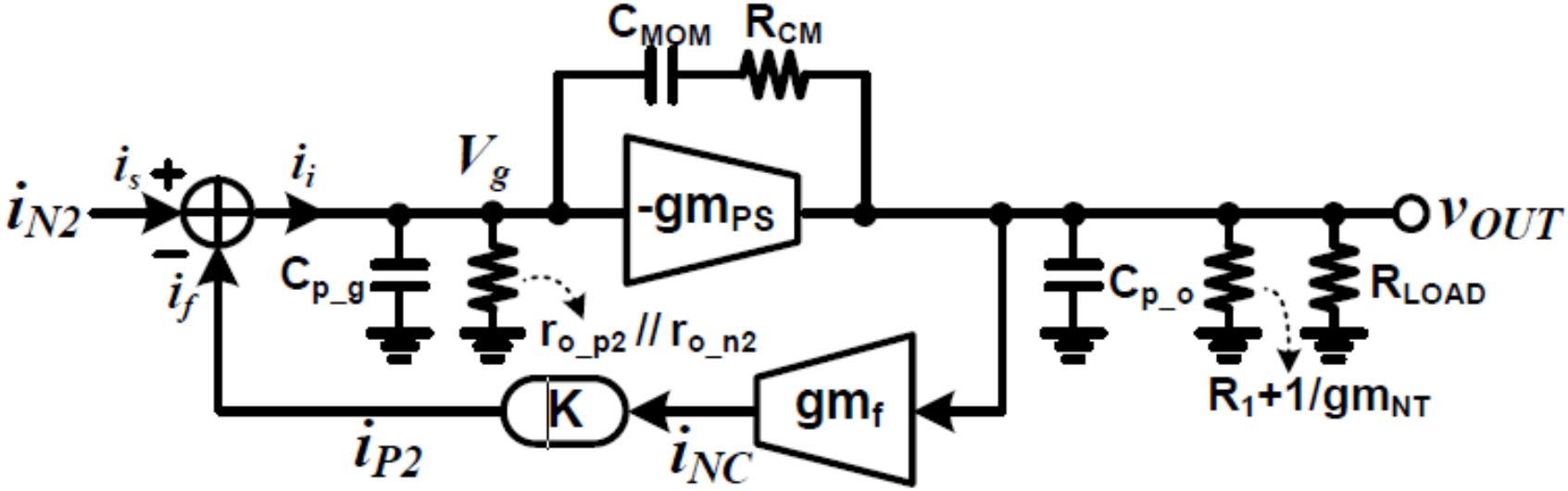


Small Signal Model

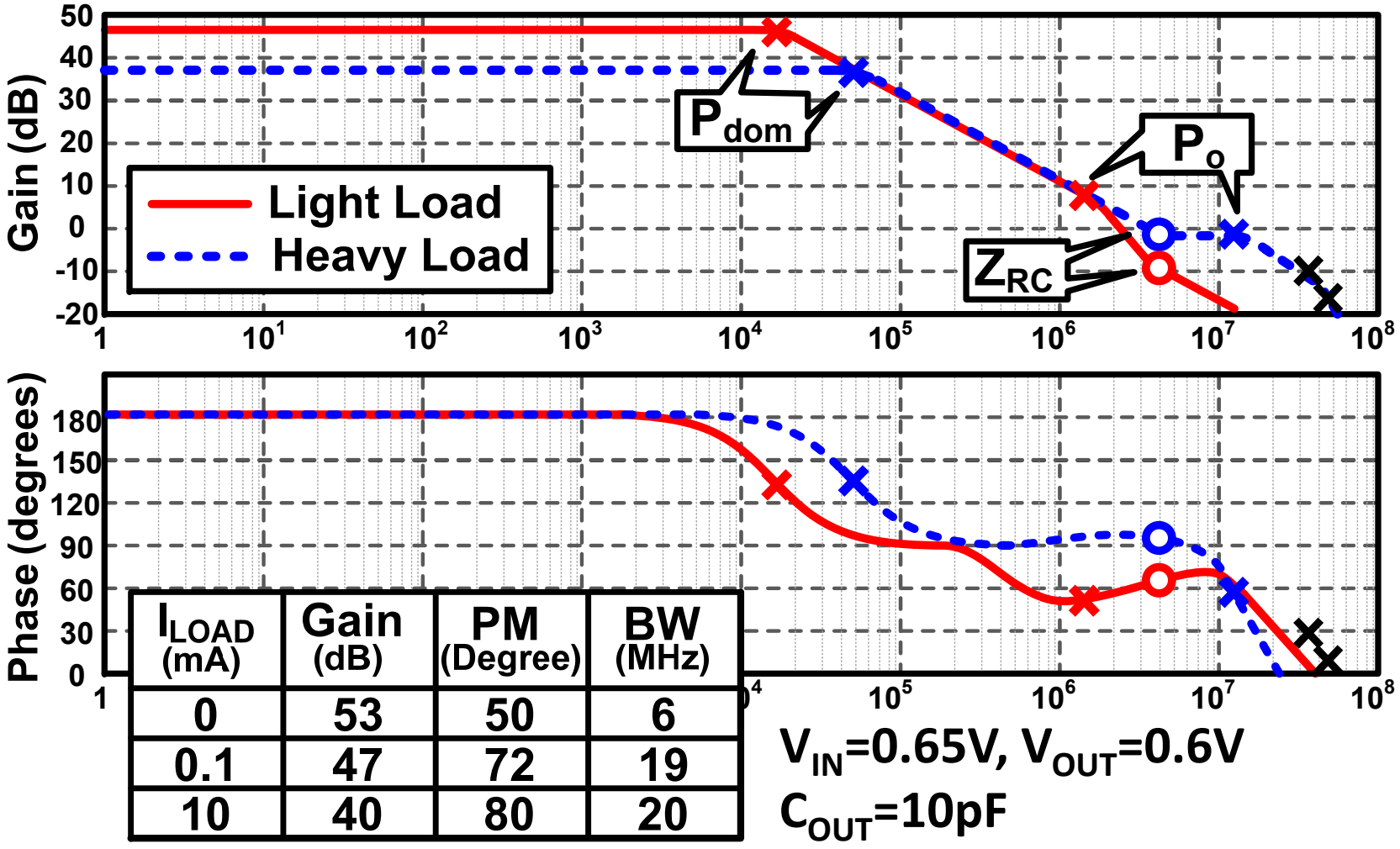


$$T(s) = A_C \frac{(\omega + Z_{RC})}{(\omega + P_{dom})(\omega + P_o)}$$

$$A_C = \frac{-gm_{ps} \cdot R_{LOAD} \cdot K}{(r_{o\_p2} // r_{o\_n2})[R_{LOAD} + (R_1 + 1/gm_{NT})]}$$



Frequency Response



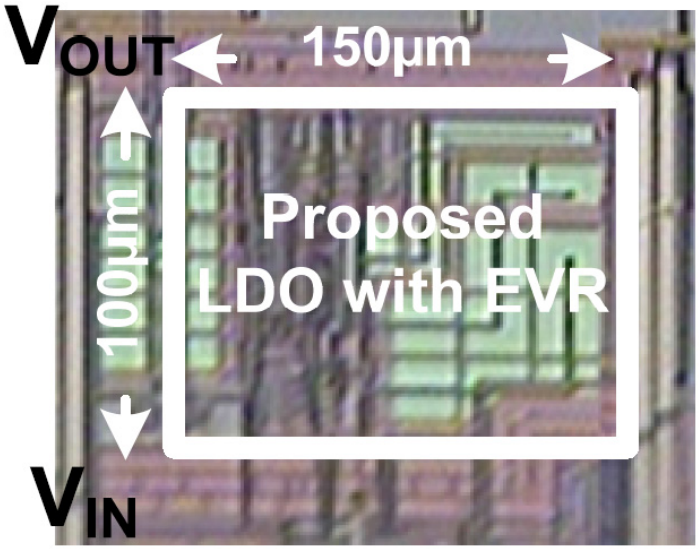
I_{LOAD} (mA)	Gain (dB)	PM (Degree)	BW (MHz)
0	53	50	6
0.1	47	72	19
10	40	80	20

V_{IN}=0.65V, V_{OUT}=0.6V

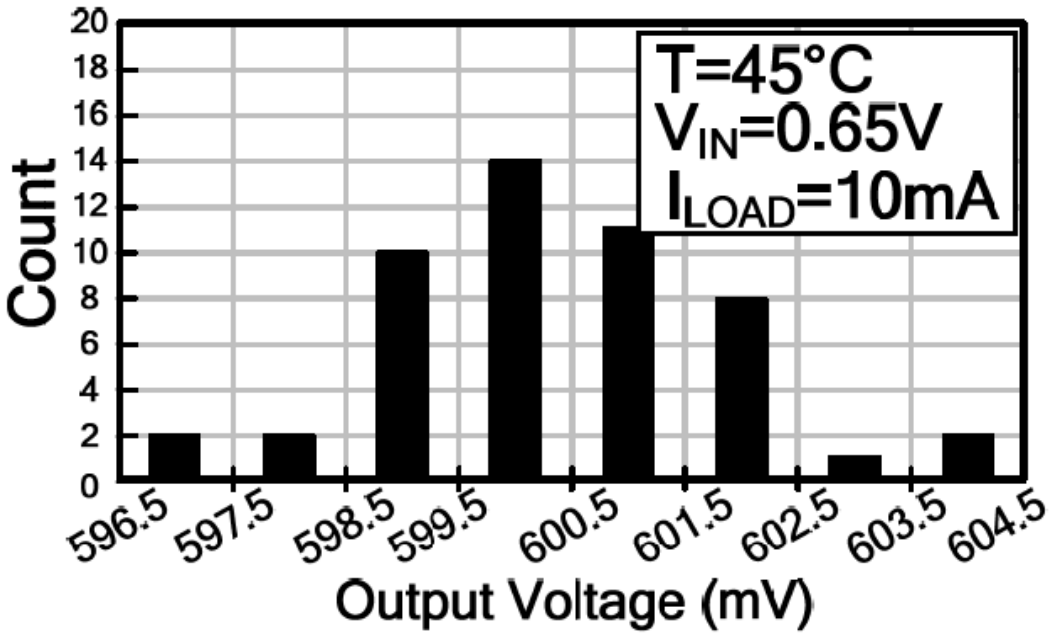
C_{OUT}=10pF

Measurement Result

- **Die Photo**

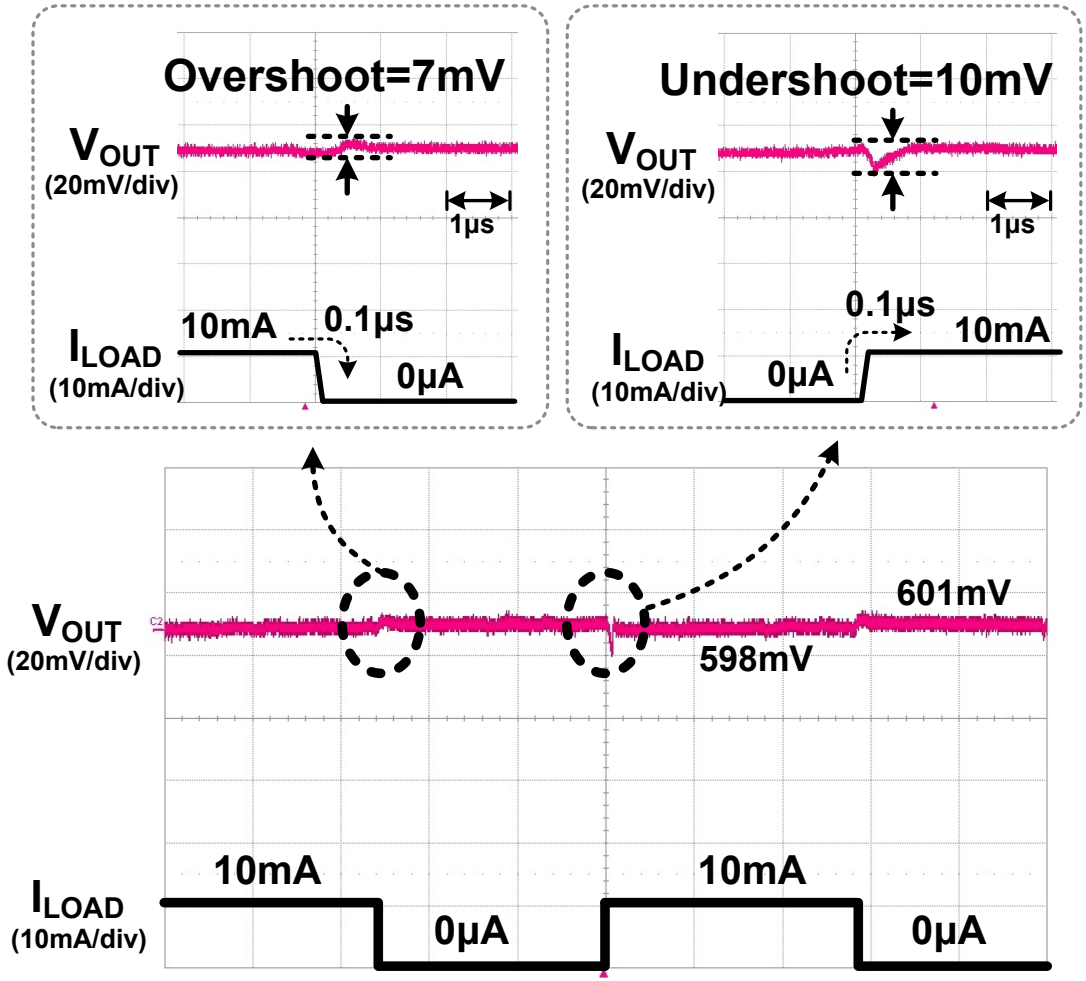


- **Output Voltage**
  (50 samples)



Load Transient Response

V_{IN}=0.65V V_{OUT}=0.6V C_{OUT}=10pF



Performance Summary

	Proposed	[5] LDO	[3] Voltage Reference	[4] Voltage Reference	unit
Technology	21nm CMOS	90nm CMOS	32nm FinFET	0.16μm CMOS	-
Voltage Reference	Embedded	#Not implement	-	-	-
Supply Voltage	0.65~0.9	0.75~1.2	0.9	1.1V	V
Supply Current	5	8	14	1.4	μA
Output Voltage	0.6	0.5~1	0.54	0.944	V
Output Capacitor	<100	<50	N/A	N/A	pF
Load Range	0~10	0~100	No	No	mA
Line Regulation	16	3.78	N/A	N/A	mV/V
Load Regulation	0.5	0.1	No	No	mV/mA
TC	30	N/A	560	30	ppm/°C
Area	0.015	0.019	0.016	0.0025	mm^2
#Need extra buffer with capacitor to bias reference voltage					

Conclusions

- Voltage reference and error amplifier are merged to realize voltage regulator.
- Low temperature coefficient of 30ppm/°C.
- Driving capability of 10mA.
- The proposed EVR technique for LDO can be applied at the low voltage condition.
- The output voltage is regulated at 0.6V when input voltage is from 0.90V to 0.65V.

Thanks for your attention

A 0.65ns-Response-Time 3.01ps FOM Fully-Integrated Low-Dropout Regulator with Full-Spectrum Power-Supply-Rejection for Wideband Communication Systems

Yan Lu, Wing-Hung Ki and C. Patrick Yue

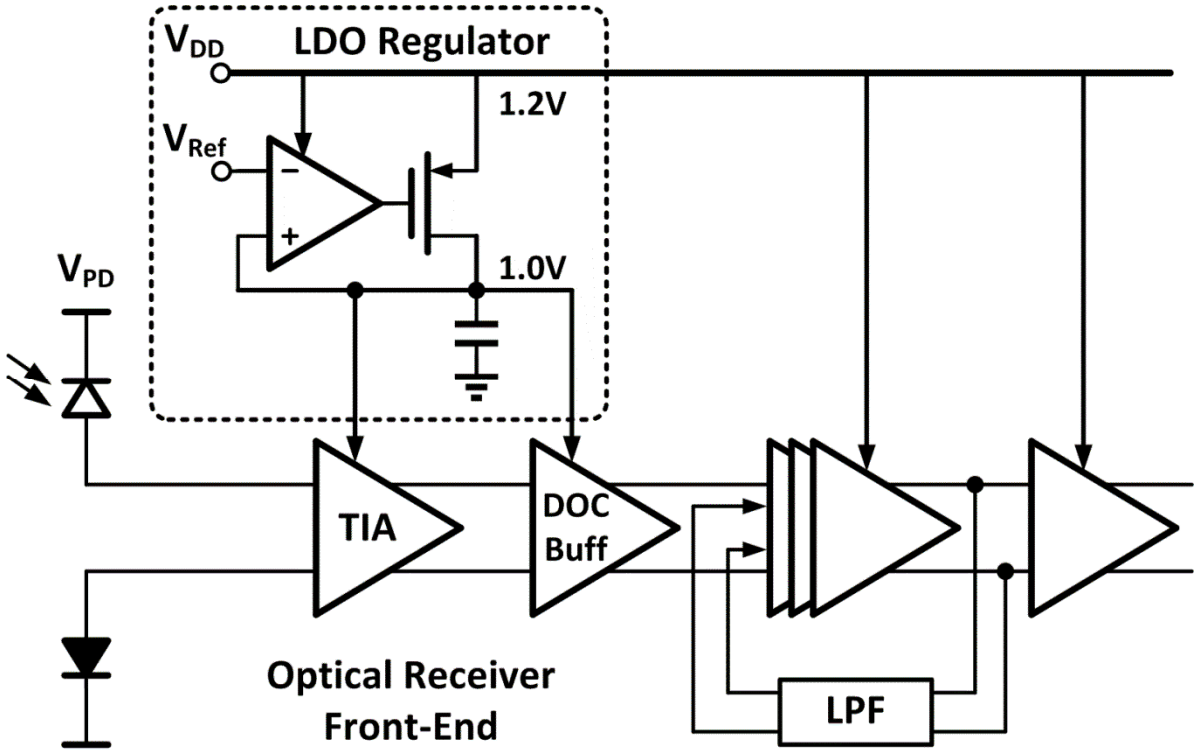
Outline

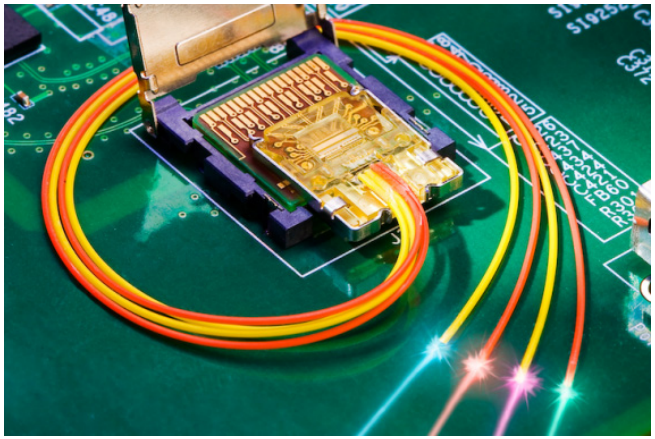
- Motivations and Requirements
- Design Considerations
  - Dominant Pole Considerations
  - Flipped-Voltage-Follower (FVF)
  - Buffer Impedance Attenuation (BIA)
- Proposed Tri-Loop Low-Dropout Regulator (LDO)
  - Loop Analyses
  - Simulation Results
  - Measurement Results
- Comparison and Conclusions

Motivations

- Fully-integrated and area-efficient low dropout regulators (LDOs) are highly desirable for point-of-load power delivery.
- LDOs with power supply rejection (PSR) up to GHz range are in demand for wideband communication systems.

[Harwood ISSCC 12]
[Takemoto ISSCC 13]





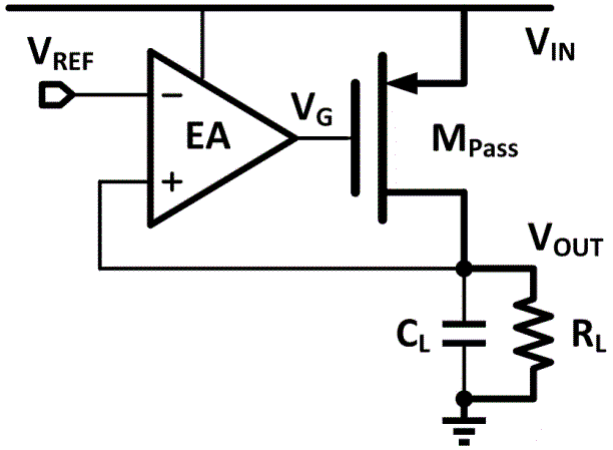
Light Peak Module - Intel

LDO Requirements

- To make a comparison, a figure-of-merit (FOM) of speed is defined as

$$\text{FOM} = T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}}$$ [Hazucha JSSC 05]

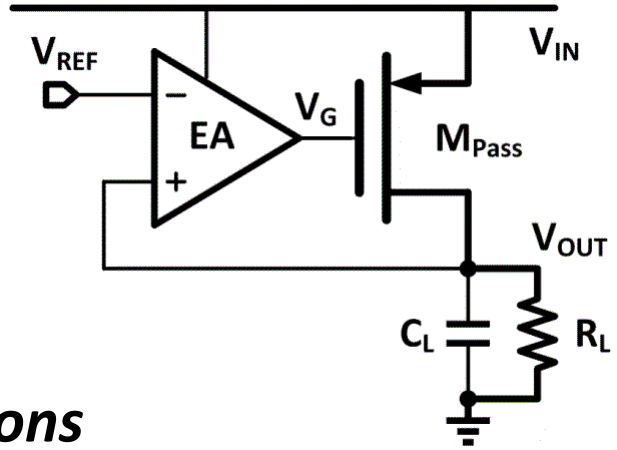
  - Fast transient response
  - Small quiescent current (I_Q)



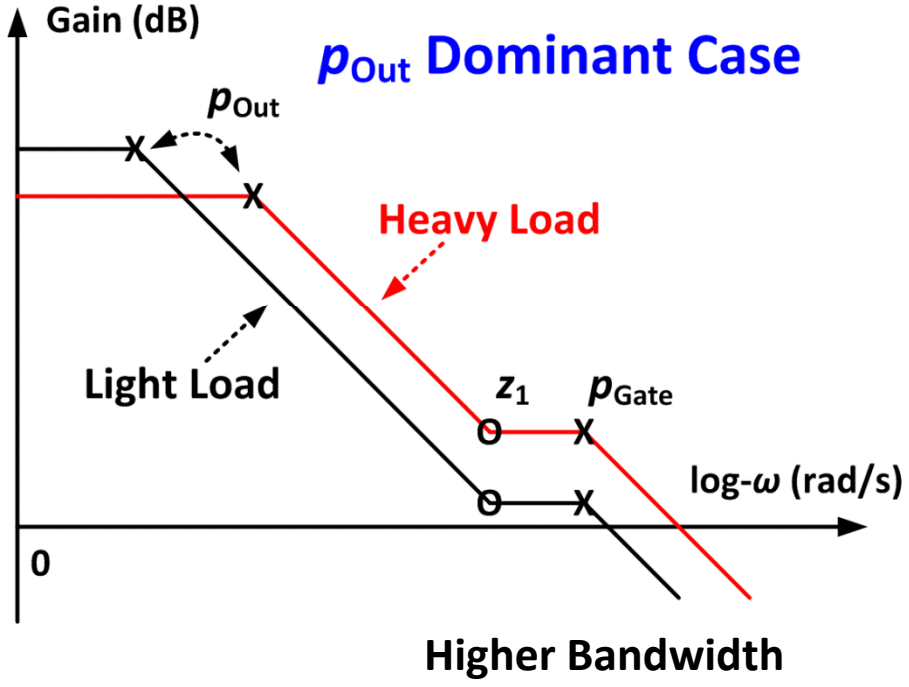
- Good PSR
- Area-efficient and scalable with process

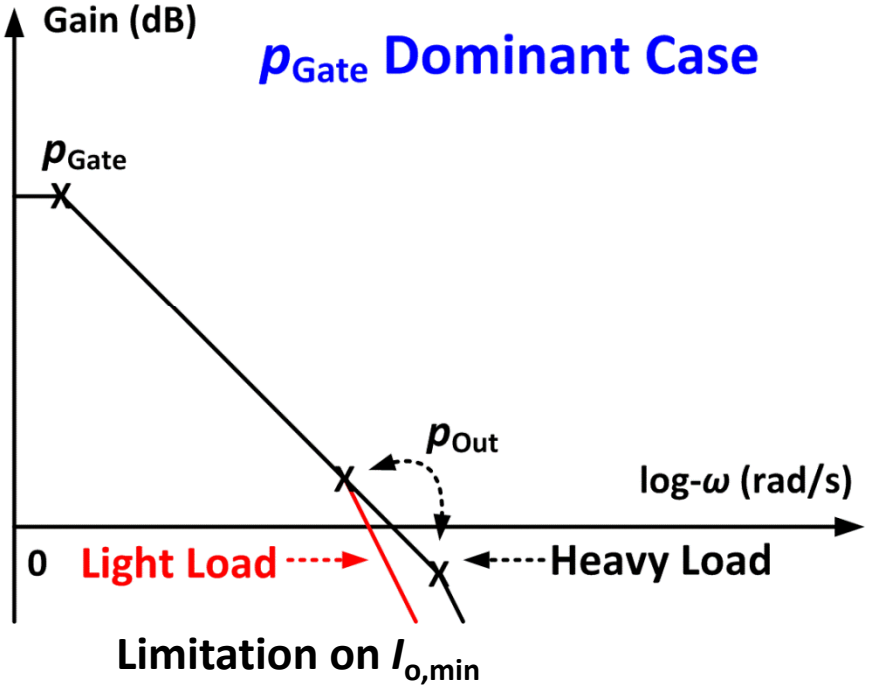
Dominant Pole Considerations

- There are at least two LF poles in an LDO:
  - p_{Gate}: Pole at the Gate of the Power MOS
  - p_{Out}: Pole at the Output

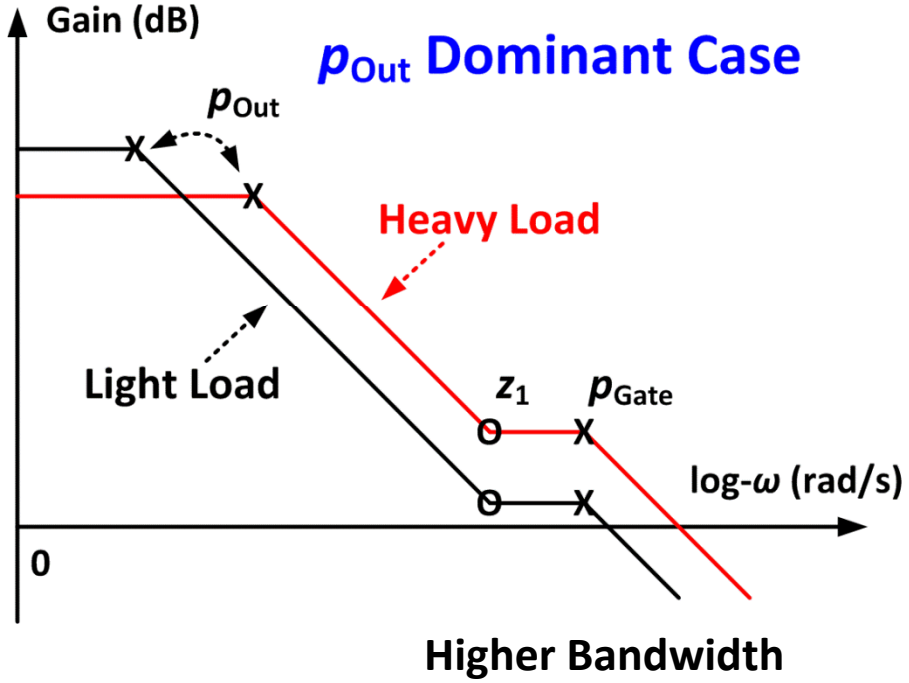


p_{Out} location would shift with load conditions

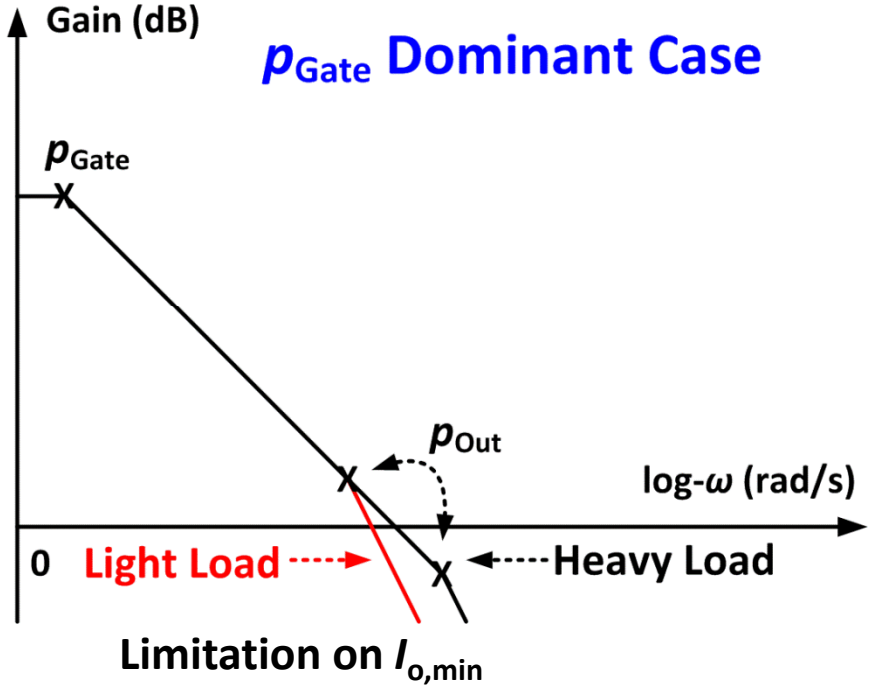




Dominant pole	p_{Out}	p_{Gate}
Process Scaling	Yes	No
Limit on $I_{o,min}$	No	Yes
UG Freq.	√	×
Transient ΔV_{OUT}	√	×
PSR	√	×
I_Q	Larger	Smaller



Higher Bandwidth



Limitation on $I_{o,min}$

LDOs with Off-/On-Chip Capacitor

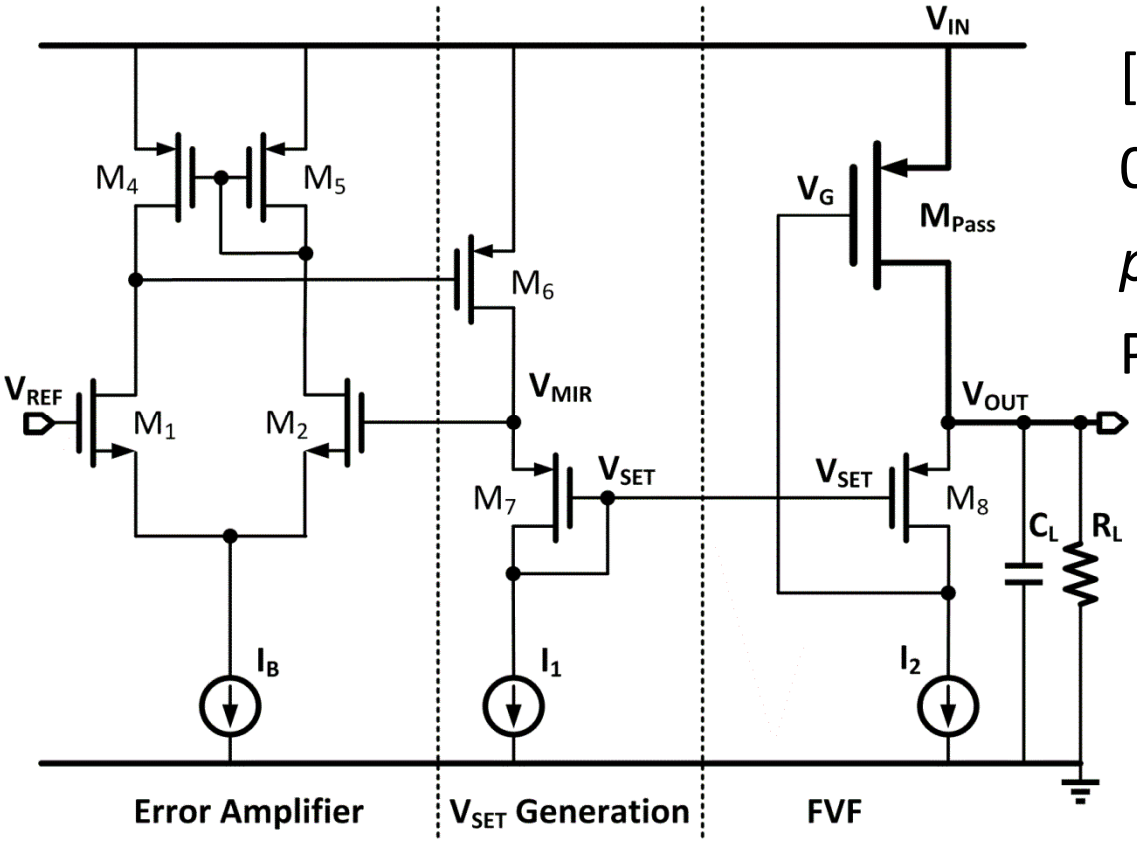
- LDOs with Off-Chip µF range Capacitor
  - Off-chip cap is conventionally added for filtering
  - Dominant pole located at the output node
  - Small load transient glitches
  - High PSR

- LDOs with On-Chip sub-nF range Capacitor
  - Dominant pole at the internal node (in previous designs)
  - Large undershoot and overshoot during load transient
  - Poor PSR

So, improving the PSR and transient performances of the fully-integrated LDO is our key design goal.

Schematic of the FVF Topology

- **Basic idea**: Use the p_{Out} dominant case with advanced process, push the internal poles to be higher than the UGF.
- **Technique**: Flipped Voltage Follower (FVF)



[Man TCAS-I 08]

0.35µm CMOS

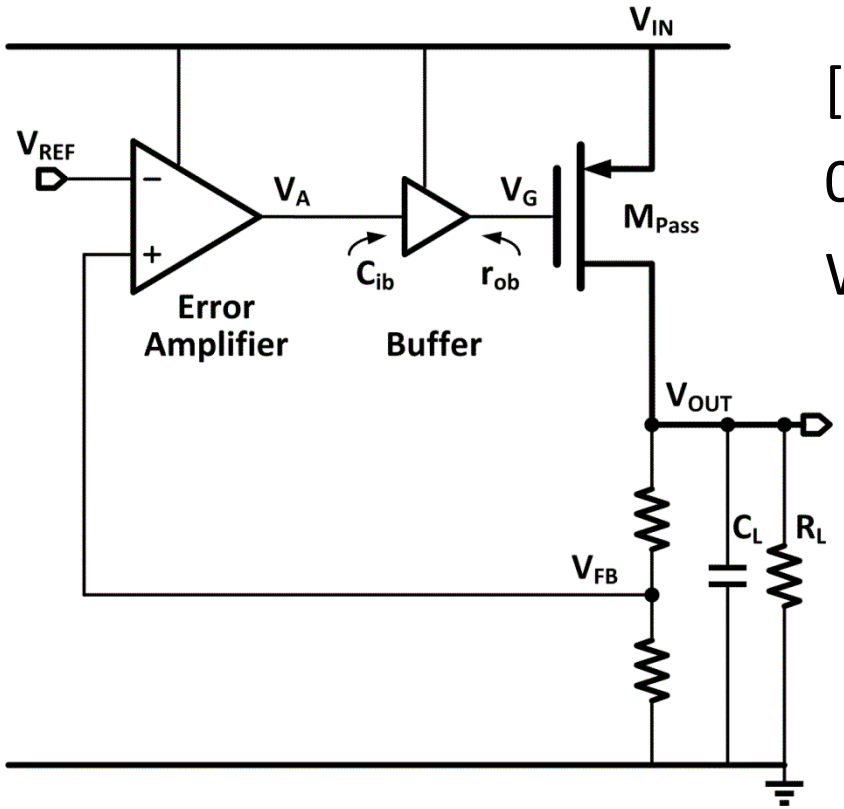
p_{Gate} Dominant

Poor DC Regulation

Schematic of the BIA Topology

- **Basic idea**: Use the p_{Out} dominant case with advanced process, push the internal poles to be higher than the UGF.
- **Technique**:

Buffer Impedance Attenuation (BIA)



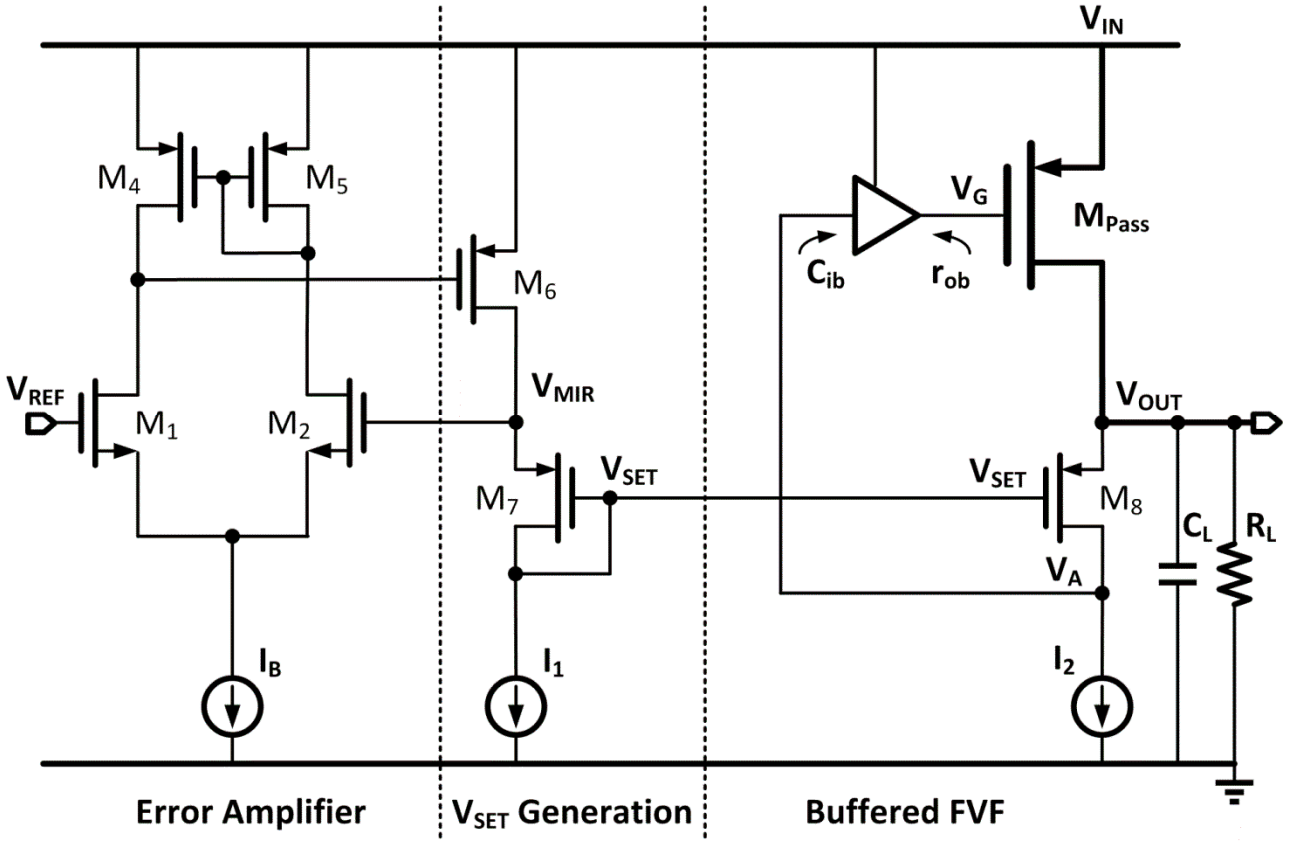
[Al-Shyoukh JSSC 07]

0.35µm CMOS

With 1µF Capacitor

Schematic of the FVF + BIA Topologies

- **Basic idea**: Use the p_{Out} dominant case with advanced process, push the internal poles to be higher than the UGF.
- **Techniques**: Flipped Voltage Follower (FVF)
  Buffer Impedance Attenuation (BIA)



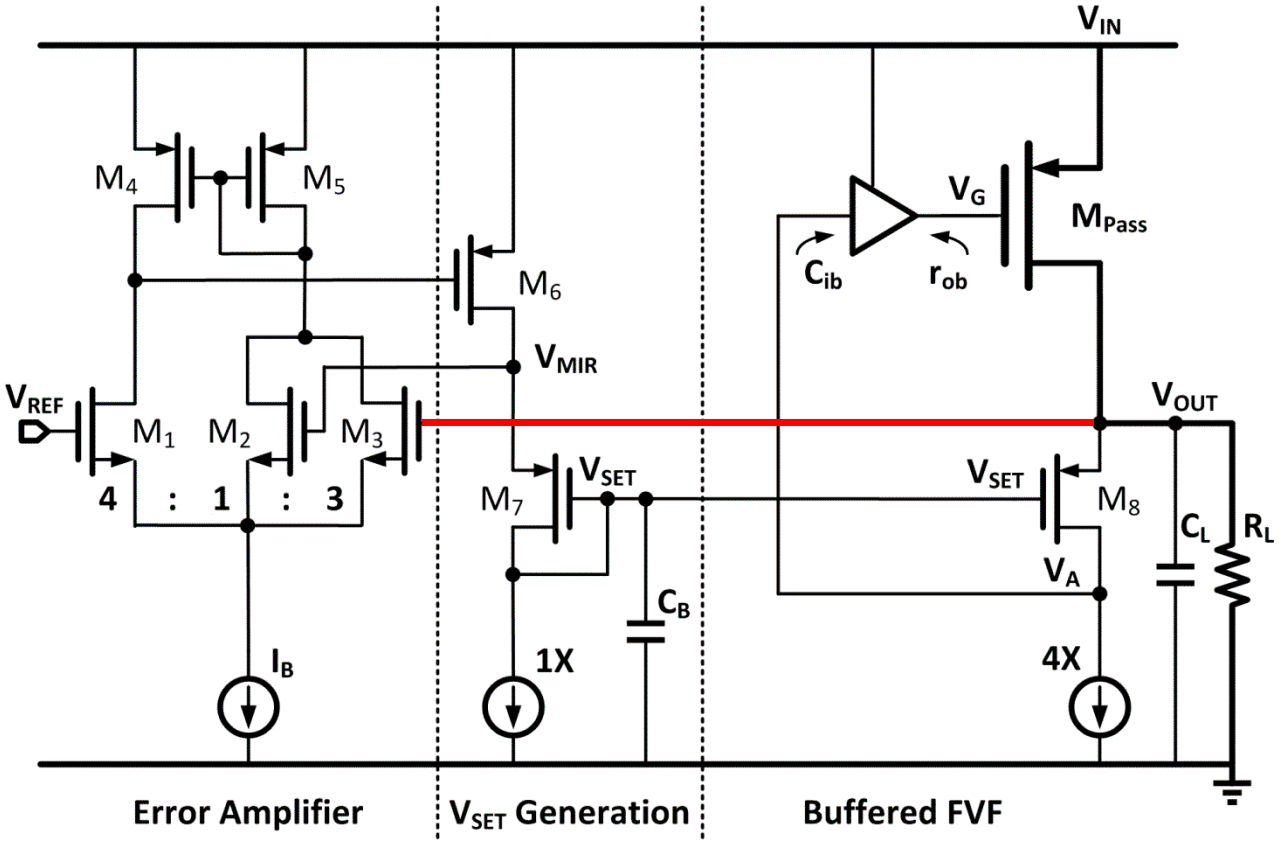
65nm CMOS

p_{Out} Dominant

Poor DC Regulation

Schematic of the Proposed Tri-Loop LDO

- **Techniques**: Flipped Voltage Follower (FVF) and Buffer Impedance Attenuation (BIA)
- **Proposed 3-Input Error Amplifier (EA), and Tri-Loop Topology**



65nm CMOS

p_{Out} Dominant

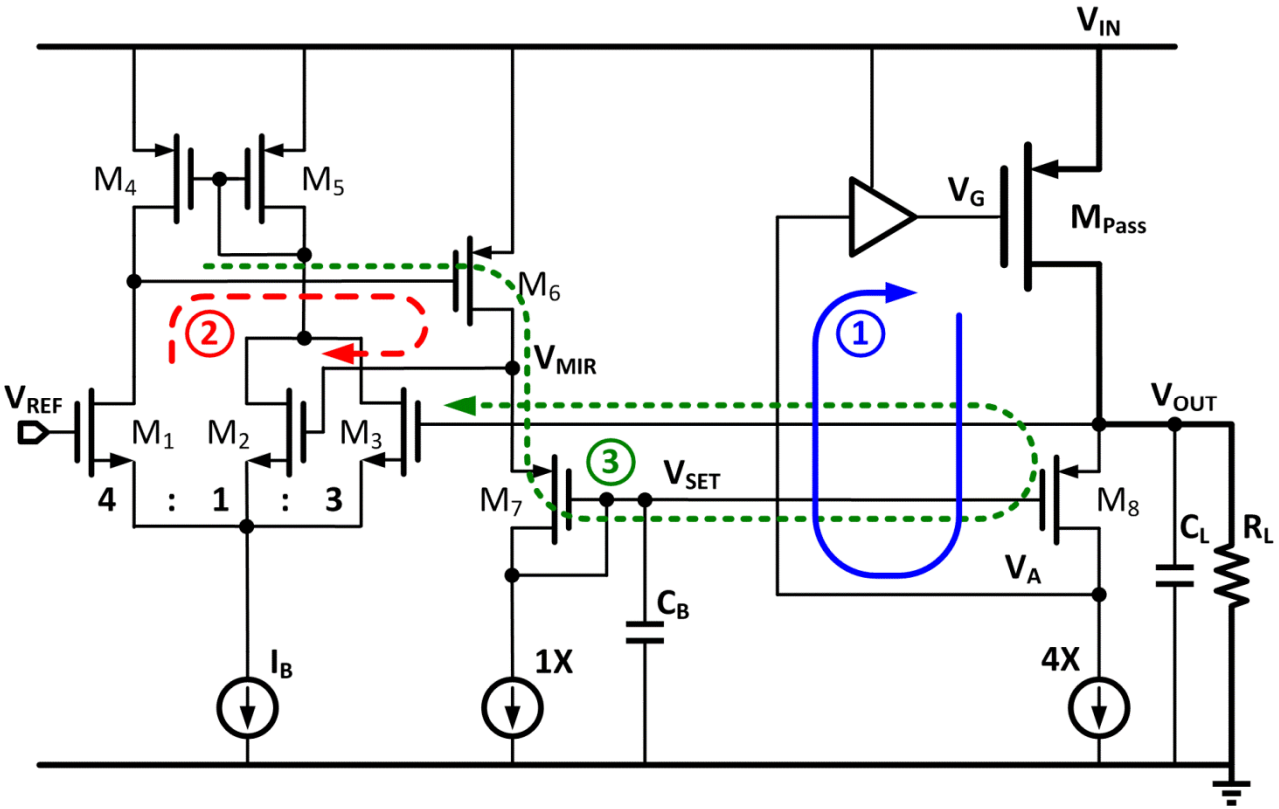
Improved DC Reg.

140pF On-Chip Cap

50µA I_Q

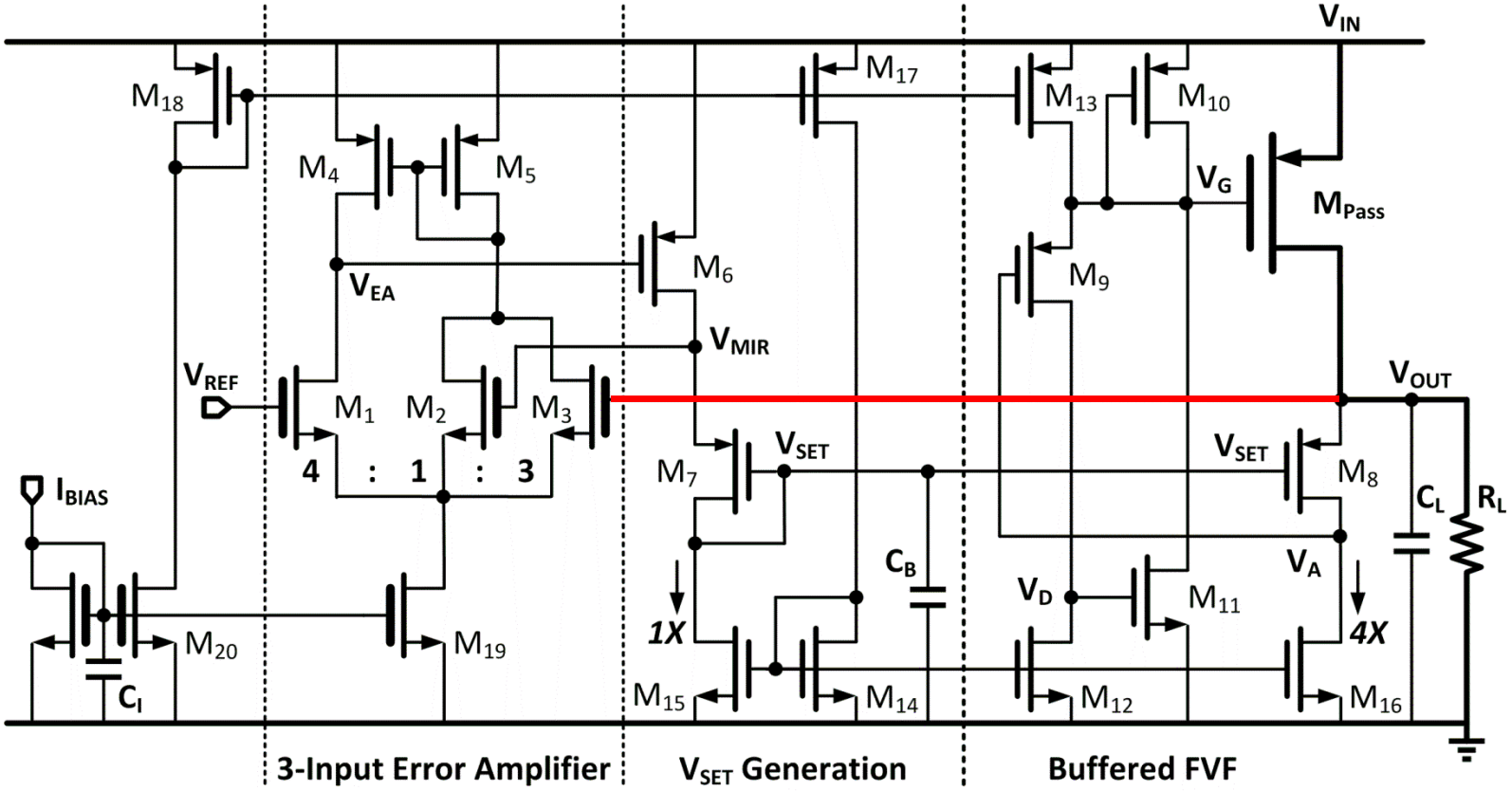
Tri-Loop in the Proposed LDO

- **Loop-1**: an ultra-fast low-gain loop with p_{Out} being its dominant pole and p_{Gate} be pushed to GHz range by BIA technique;
- **Loop-2**: a slow loop that generates V_{MIR} andV_{SET};
- **Loop-3**: feed V_{OUT} back to the EA to improve the DC accuracy.



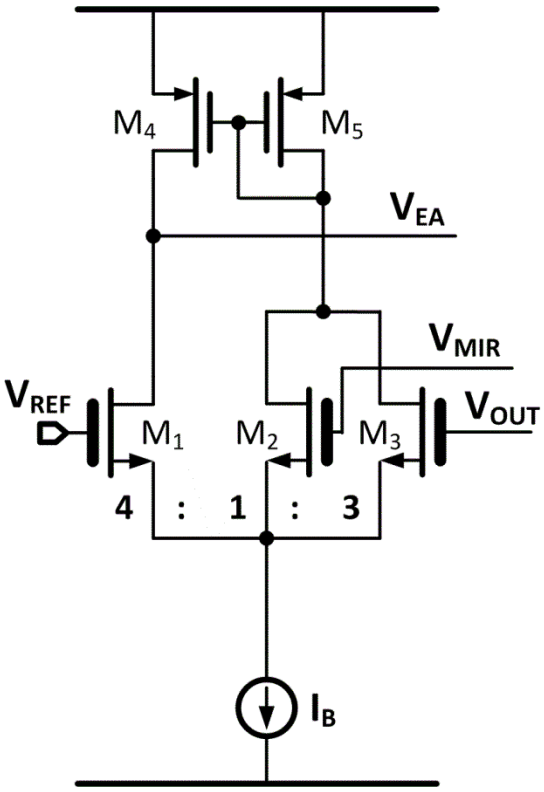
Schematic of the Proposed Tri-Loop LDO

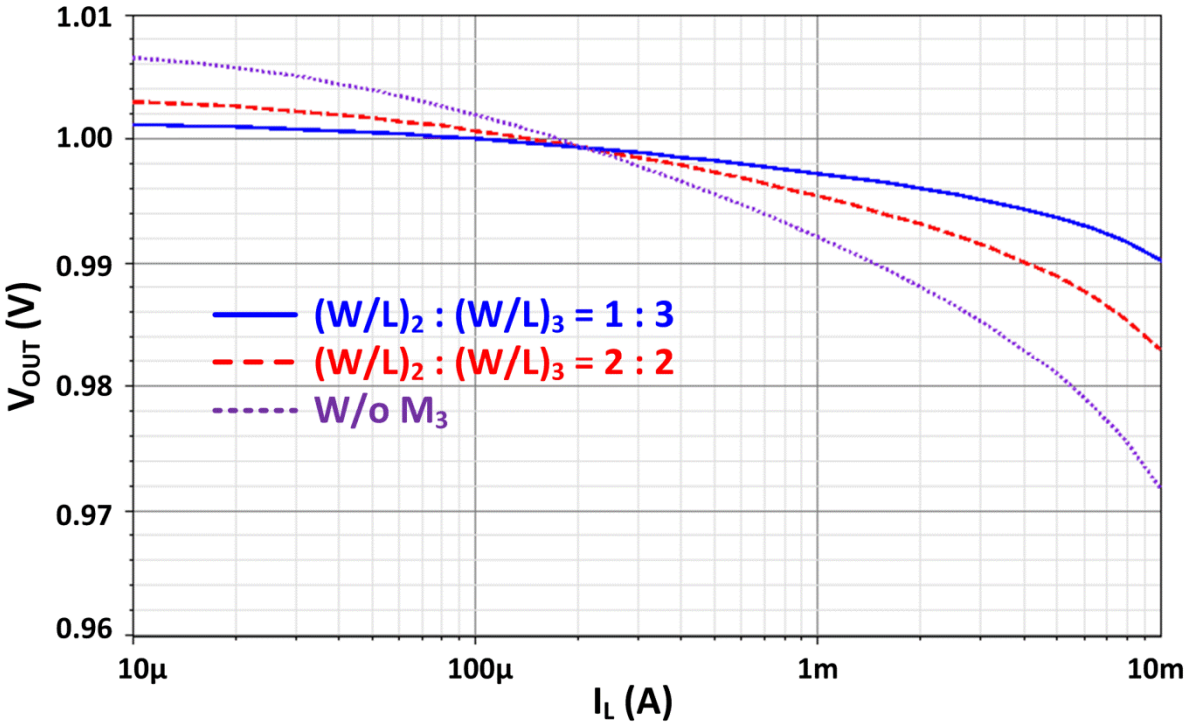
- **Techniques**: Flipped Voltage Follower (FVF) and Buffer Impedance Attenuation (BIA)
- **Proposed 3-Input Error Amplifier (EA), and Tri-Loop Topology**



Effect of the Tri-Loop Input Stage

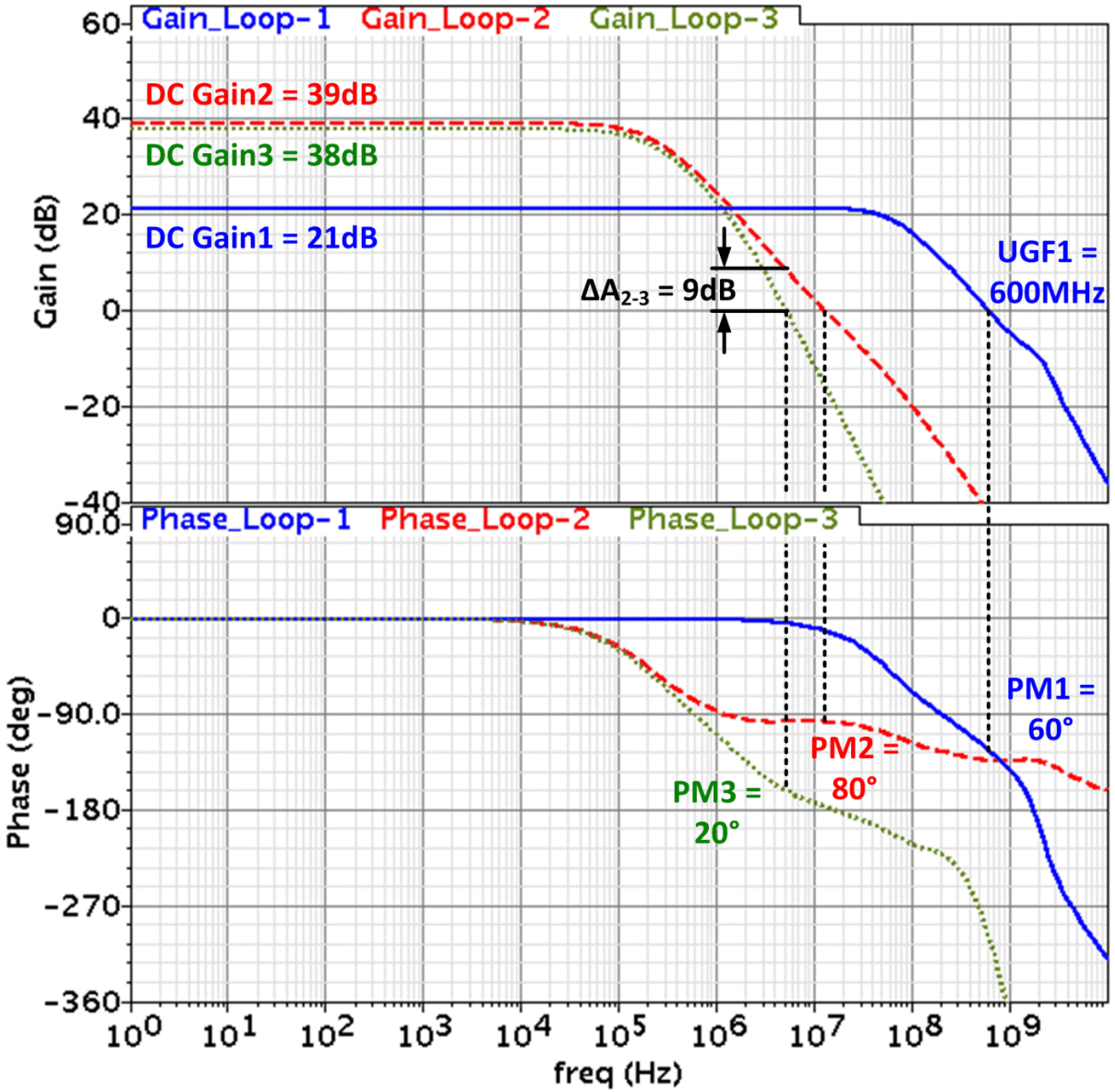
- Improved DC Accuracy with $(W/L)_2 : (W/L)_3 = 1 : 3$





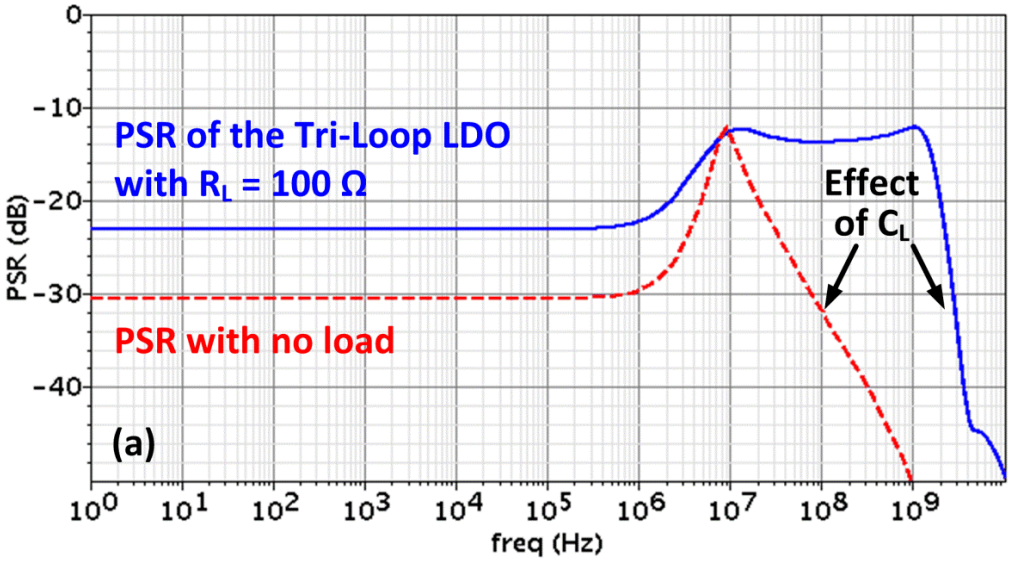
Simulated Bode Plots of Loop-1, 2, 3

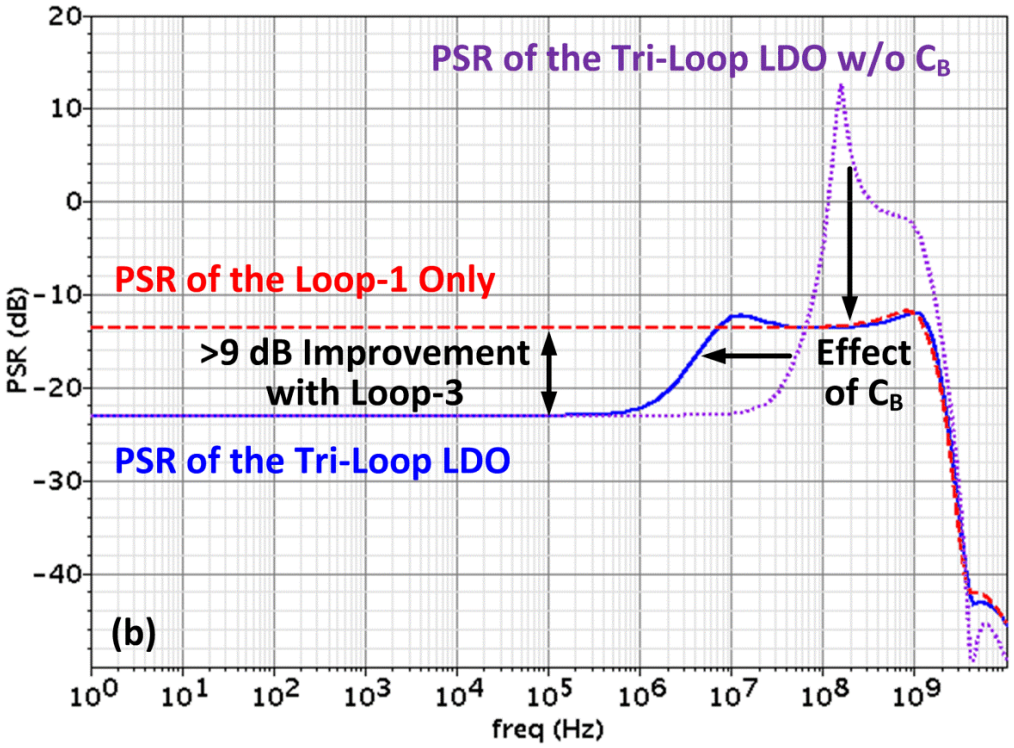
- V_{IN} = 1.2V
- V_{OUT} = 1.0V
- R_L = 100Ω



Simulated PSR

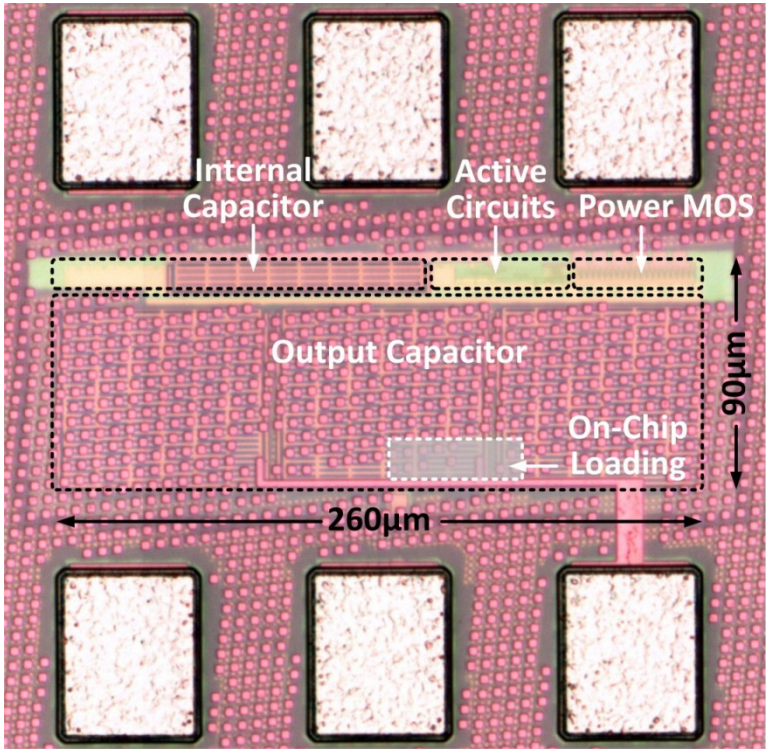
- V_{IN} = 1.2V
- V_{OUT} = 1.0V
- R_L = 100Ω

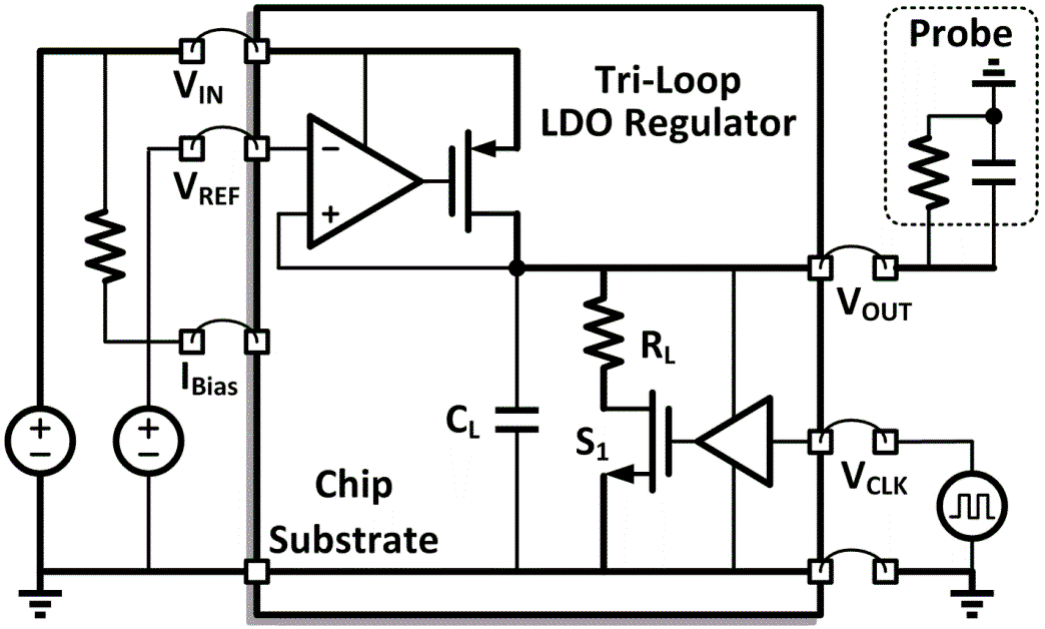




Chip Micrograph of the LDO in 65nm

- Effective Area: $90 \times 260\ \mu m^2$ (with on-chip loading)
- Total on-chip capacitance: 140pF
  (stacked MOS and MIM capacitors)





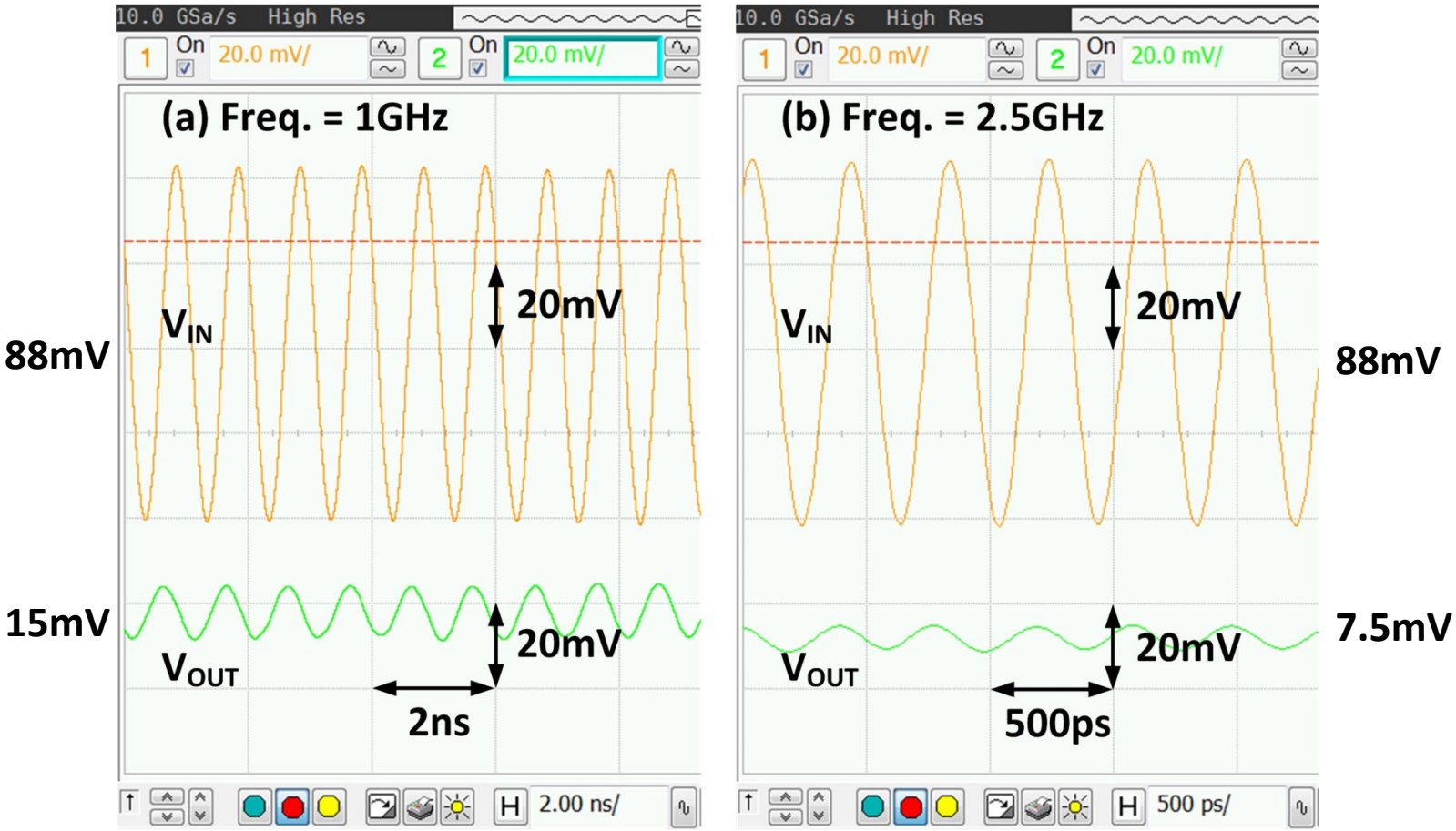
Ultra Fast Transient Response

- Rising/Falling edges of the load : < 200ps (0µA to 10mA)
- I_Q: 50µA; C_{Total}: 140pF; ΔV_{OUT}: 43mV (undershoot)
- Response time T_R: 0.6ns
- FOM: 3.01fs

$$\text{FOM} = T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}}$$

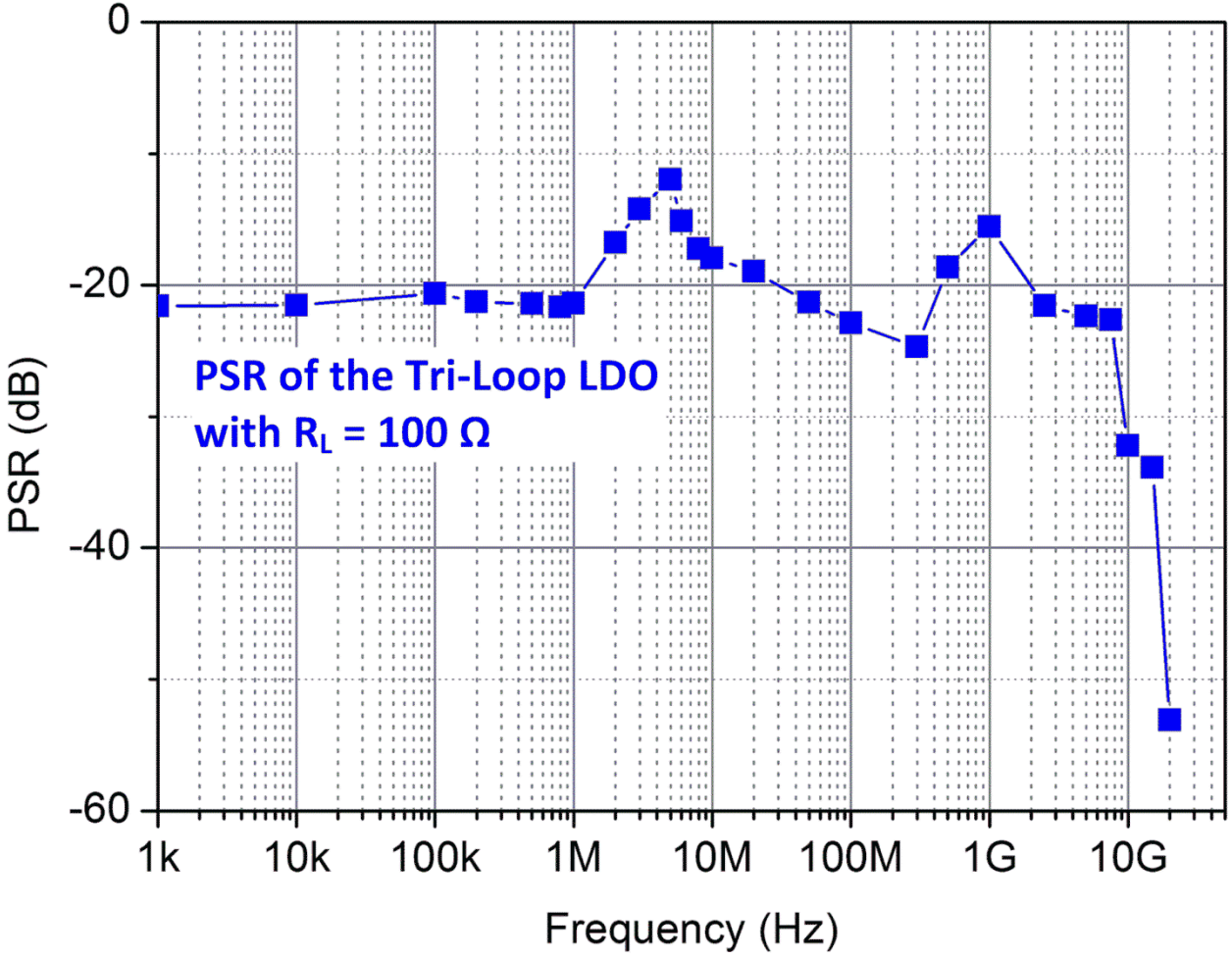
Measured PSR @ 1GHz and 2.5GHz

- V_{IN} = 1.2V, V_{OUT} = 1.0V, R_L = 100Ω



Measured PSR up to 20GHz

- V_{IN} = 1.2V, V_{OUT} = 1.0V, R_L = 100Ω
- -21.4dB @ 1MHz
- -12dB @ 5MHz
- -15.5dB @ 1GHz



Comparison with the State-of-the-Art LDOs

Publication	P. Hazucha JSSC 2005	J. Guo JSSC 2010	J. Bulzacchelli JSSC 2012	This Work
Output Cap.		**On-chip**		
Technology	90nm	90nm	45nm SOI	**65nm**
V_{OUT}	0.9V	0.5 to 1V	0.9 to 1.1V	**1V**
Drop out	300mV	200mV	85mV	**150mV**
I_Q	6mA	8µA	12mA	**50µA**
Io,max	100mA	100mA	42mA	**10mA**
Capacitance	600pF	50pF	1.46nF	**140pF**
PSR	N/A	0dB @1MHz	N/A	**-15.5dB @ 1GHz**
ΔV_{OUT} @T_{edge}	90mV @100ps	114mV @100ns	N/A	**43mV @200ps**
Load Reg.	90mV	10mV	3.5mV	**11mV**
T_R	0.54ns	N/A	0.288ns*	**0.6ns**
FOM	32ps	N/A	62.4ps*	**3.01fs**

* Simulated result

Conclusions of the Tri-Loop LDO

- A tri-loop LDO regulator with buffered FVF is proposed and fully-Integrated in 65nm CMOS.
- Sub-ns T_R is measured with on-chip loading, which has a step change between 0 and 10mA within 200ps.
- PSR is measured to be <-12dB from DC to 20GHz.
- The 3.01fs FOM is achieved as compared to the published LDO regulators.

Thank You for Your Attention!

Yan LU, 2014